Digital Front-End Electronics for the Neutron Detector NEDA

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***Abstract*—This paper presents the design of the NEDA (Neutron Detector Array) electronics, a first attempt to involve the use of digital electronics in large neutron detector arrays. Starting from the front-end modules attached to the PMTs (PhotoMultiplier Tubes) and ending up with the data processing workstations, a comprehensive electronic system capable of dealing with the acquisition and pre-processing of the neutron array is detailed. Among the electronic modules required, we emphasize the front-end analog processing, the digitalization, digital pre-processing and communications firmware, as well as the integration of the GTS (Global Trigger and Synchronization) system, already used successfully in AGATA (Advanced Gamma Tracking Array). The NEDA array will be available for measurements in 2016.**

***Index Terms*—Digital systems, front-end electronics, neutron detectors, neutron-gamma discrimination.**

Manuscript received June 16, 2014; revised December 22, 2014; accepted January 06, 2015. Date of publication February 18, 2015; date of current version June 12, 2015. This work was supported by the Generalitat Valenciana, Spain, under grant PROMETEO/2010/101. Some authors were supported in part by INFN, Italy, and by the Spanish MINECO under grants AIC-D-2011-0746, FPA2011-29854, and FPA2012-33650. The Swedish Research Council, the Scientific and Technological Research Council of Turkey (TUBITAK), and the UK STFC also provided support.

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Digital Object Identifier 10.1109/TNS.2015.2392159

I. Neutron Detector Arrays with Digital Electronics

RESEARCH on Nuclear Structure of exotic nuclei has led physicists to use high-resolution gamma spectrometers coupled with neutron and charged-particle detectors in order to identify products from the nuclear reactions. Special efforts are made to obtain efficient detectors for neutron identification, with reduced neutron cross-talk, being one of the main goals for the new-generation NEDA [1]. NEDA is expected to play a major role as a neutron detector array for future experiments using high-intensity stable and radioactive ion beams coupled with the gamma-ray spectrometers AGATA [2], EXOGAM (EXOtic GAMma array detector) [3] and GALILEO [4]. Fig. 1 shows a schematic view of NEDA coupled to AGATA and the currently existing Neutron Wall [5].

The NEDA design has focused on obtaining large neutron efficiencies, low cross-talk, excellent NGD (Neutron-Gamma Discrimination) [6] and high rate capabilities. These specifications led to a detector design with large volumes of BC501-A organic scintillator combined with a geometry capable to minimize the effects of scattered neutrons. Neutron detection, while largely depending on the detector design, depends also on the electronics, requiring accurate TOF (Time-of-Flight) and PSA (Pulse-Shape Analysis) measurements to enhance the scattering rejection and NGD performance. Additionally, an advantage of BC501-A, despite its high-efficiency for neutron collection, is the capability to produce different decay components depending on the type of impinging particle. Experiments using XP4512 PMTs have shown that signals involved in the process have fast rise-times around 10 ns [7], [8], followed by an exponential decay, close to 500 ns, which involves several decay time constants. Dedicated communication links are required due to the expected maximum count rate with high-intensity ion beams, expected to be close to 50 kHz.

The dynamic range is set by the sensitivity of the PMTs at 1 V/MeVee (electron volt equivalent) while the gain is set on

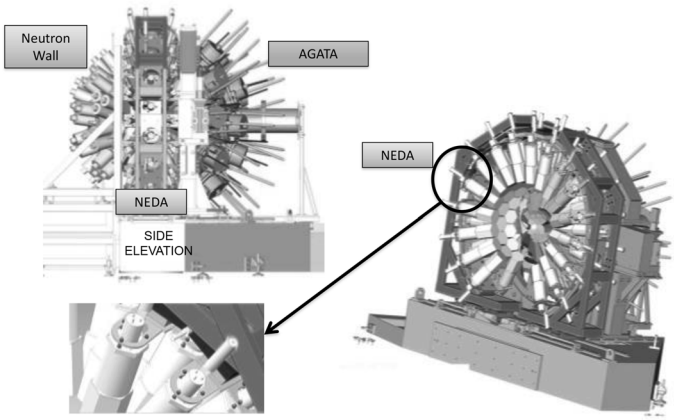

Fig. 1. Scheme of NEDA coupled with Neutron Wall and AGATA.

the front-end analog stages and the FADC (Fast Analog to Digital Conversion) Mezzanine. The interest is focused on the neutrons whose energy range is from the detection threshold, set at few tens of keVee, to a maximum energy of 8 MeVee. The desired resolution should be larger than 11 ENOB (Effective Number Of Bits) in order to obtain at least 2000 energy channels. A second point which impacts on the choice of a sampling device is the NGD performance [6], [7]. In the case of NEDA, NGD is performed both on TOF measurements and PSA algorithms. According to [6], a satisfactory discrimination based on PSA can be achieved with 10 bits and 100 Msps. However, TOF measurements demand higher sampling rates and interpolation techniques in order to achieve the desired timing resolution. In [8], it has been shown that, at least, a minimal sampling rate of 200 Msps is required together with the implementation of interpolation techniques. Summarizing the requirements for the A/D conversion, at least 11 ENOB and 200 Msps are required to achieve the desired specifications.

Regarding the specifications related to the readout protocol, most of the useful information which can be retrieved from the waveform is contained within the first 500 ns, a time which is long enough to perform PSA techniques such as charge-comparison methods or ZCO (Zero Cross-Over) [6], [7]. All the required samples within an event can be gathered in a time window of 1.25 μs. This includes as well some pre-trigger samples to calculate the baseline and a set of samples left as a safety margin. For 50 kHz/channel counting rate, and 2 bytes/sample, the estimated data throughput rises up to 25 MB/s for each channel. Table I summarizes the requirements to develop the electronics.

II. Global Electronics Layout

NEDA electronics design will be conducted in three phases. Firstly, the new digital electronics are envisaged to instrument the former Neutron Wall detector [5], consisting of 45 detectors, to which 45 more new NEDA detector modules are expected to be connected in 2015. NEDA will eventually be composed of 331 detectors [1]. The connection to AGATA and other detectors has still to be foreseen.

The electronic chain consists of the following parts: the front-end single-ended to differential converters, the NUMEXO2 (Numériseur pour EXOGAM) motherboard [9], the FADC Mezzanines [10], the LINCO2 PCIe readout interface [11], the GTS system [12] and the workstations for data acquisition and processing.

TABLE I
Requirements for Neda Electronics

Requirement	
Sampling rate	200 Msps
ENOB	> 11
Number of channels	331
Raw data throughput	25 MB/s each channel
Synchronization	Common clock derived from the GTS
Trigger system	Based on AGATA GTS

Each single detector module is readout by one single front-end electronics channel whenever a current signal is extracted from the corresponding PMT. The PMTs are connected to the single-ended to differential converter board in order to send the pulse through a 10 m cable to the NUMEXO2 digitizer. Each single-ended to differential conversion board processes a total number of 8 channels. Once the signal reaches NUMEXO2, the digitizer motherboard contains 4 FADC Mezzanines plugged onto it. These are used to perform the A/D conversion at 200 Msps with a resolution of 14-bits. Then, the digital pre-processing is carried out using Field Programmable Gate Arrays (FPGAs) inside the NUMEXO2 motherboard: a V6 (Virtex-6) and a V5 (Virtex-5). These cope with the readout and digital pre-processing for 16 channels. Firstly, a trigger algorithm based on PSA is applied in the V6 in order to reduce the events produced by gamma-rays, hence, optimizing the readout bandwidth capabilities. The trigger requests, now produced mostly by neutrons, are received and sent to the GTS, waiting for a validation or rejection. The V5 includes a Power PC (PPC) embedded processor containing an embedded Linux OS, which is utilised to cope with the slow-control (SPI/I2C) and the communication management tasks such as the TCP/IP, GTS leaf and PCIe protocol.

Regarding the readout capabilities based on event window and count rate, each NUMEXO2 deals with 400 MB/s (16×25 MB/s), requiring an optical link capable of transmitting a minimal data rate of 3.2 Gbps for each digitizer. Fig. 2 illustrates the global electronic layout for 45 detectors.

The estimated power consumption of the digitizer is $\sim$ 100 W.

III. The Parts

In the following paragraphs, the different parts of the NEDA front-end electronics are described. Table II has been attached in order to show the boards which are particular for NEDA electronics and the elements which are shared with other detectors.

A. Single-ended to differential converter and HDMI cable

Given that fast pulses, involving rise-times faster than 10 ns, and the 10-m distance between NUMEXO2 and the detectors, it was preferred to drive the signals in differential mode in order to reduce the noise contributions and interferences. Therefore, a single-ended to differential conversion module is placed near to the detectors, connecting the PMTs to the aforementioned module by using short coaxial cables.

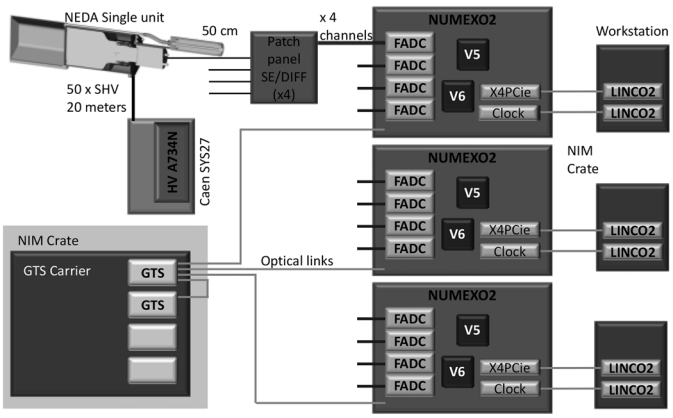

Fig. 2. Global electronics layout for NEDA involving the use for 45 detectors.

TABLE II
HARDWARE ELEMENTS AND SYNERGIES

Element	Shared with
Single-ended to differential board	Particular for NEDA
HDMI cable	EXOGAM2
FADC Mezzanine	EXOGAM2
NUMEXO2	EXOGAM2
GTS boards	EXOGAM2, AGATA
LINCO2 boards	AGATA

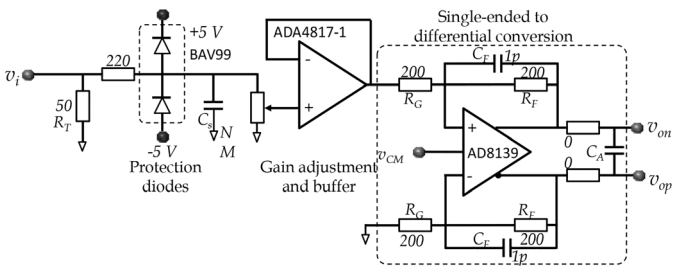

Fig. 3. Front-end single-ended to differential board schematics.

The board is provided with 4 channels, each containing a single-ended coaxial input, differential output and a monitor single-ended output for testing purposes. The conversion is performed with the low-noise operational amplifier *ADA4817* and the fully-differential *AD8139*. Additionally, the circuit contains also protection circuitry against high-voltage peaks by means of low-capacitance BAV99 diodes (< 1.5 pF), and a potentiometer used to reduce and adjust the gain. An optional capacitor can be mounted in case of a desired signal shaping. Fig. 3 depicts the schematic for a single channel.

Regarding the transmission cable selection between the single-ended to differential board and NUMEXO2, a dedicated testbench has been developed aimed to qualify several models in terms of bandwidth, crosstalk and EMI (ElectroMagnetic Interference). Table III summarizes the results obtained for the evaluated candidates. The bandwidth considers also the front-end electronics board, being the result of the ratio between the measured output and input. Crosstalk tests have been performed using square waveforms with adjustable edge times of 1 V_{pp}. Table I shows the results for 2.5 ns rise times. Finally,

TABLE III
CABLE TESTS AND RESULTS

Element	BW	Crosstalk	EMI
MDSM	--	43.8 mV	--
HDMI	70 MHz	4.18 mV	1.07 V
HDMI 1.4 Infinite	120 MHz	3.82 mV	356 mV
PoCL-Lite	35 MHz	8.02 mV	6.25 V

EMI was measured by injecting 1 kV pulses at 50 Hz through a covering foil paper around the external cable coating.

B. The NUMEXO2 Pre-processing Card

NUMEXO2 [9] is the core of the NEDA front-end electronics, being designed in collaboration with EXOGAM2, thus aiming to reduce time and resources. NUMEXO2 functions can be summarized as: A/D conversion, data pre-processing, connection to the GTS system and data readout for 16 channels. Physically, the system is composed of a motherboard and the set of 4 FADC Mezzanines. The measured total power consumption of NUMEXO2 is 100 W (6.25 W/ch), from which 25 W are consumed in the FADC Mezzanines.

Three clock sources are used in NUMEXO2: A local oscillator, the recovered clock obtained from the GTS tree and a third option based on an external clock source through the front panel. During the booting process and also, in case that NUMEXO2 works in a standalone mode, it can select the local oscillator as the main clock source. However, as several NUMEXO2 cards are involved in the experiments, it is required to use of the recovered GTS clock as the main source in order to synchronize the clocks for the all FADC Mezzanines and motherboard. An exception is the case of the PPC inside the Virtex-5, which is always clocked from the local oscillator source.

C. The FADC Mezzanines

Each FADC Mezzanine digitizes 4 channels. Additionally, due to the collaboration with EXOGAM2 HP-Ge spectrometer, an ADC with higher resolution is required, with at least 11.3 ENOB, leading to the selection of the dual FADC *ADS62P49* as the core device for this application, with 14-bit and 250 Msps [10].

According to the resolution specifications, the rest of devices such as the jitter cleaner *LMK03001C*, low-noise analog coupling stages based on fully-differential amplifiers *AD8139*, Digital-to-Analog converters (DACs), power regulators and connectors have been selected. The FADC Mezzanine block diagram is depicted in Fig. 4.

The analog input stage coupled with the FADC is the most critical in terms of noise after the selection of the proper FADC and jitter cleaner. Additionally, extra offsets are added in order to take full advantage of the FADC dynamic range, allowing the acquisition of both unipolar and bipolar signals. Following an in-depth study, the coupling is performed by means of *AD8139* Fully-Differential Amplifiers (FDAs). Since the noise performance of the *AD8139* is shown optimal for unitary gains, the strategy to obtain an attenuation factor without leading to instability can be achieved by adding a T-divider between 2 *AD8139*-based stages, allowing preservation of the noise performance

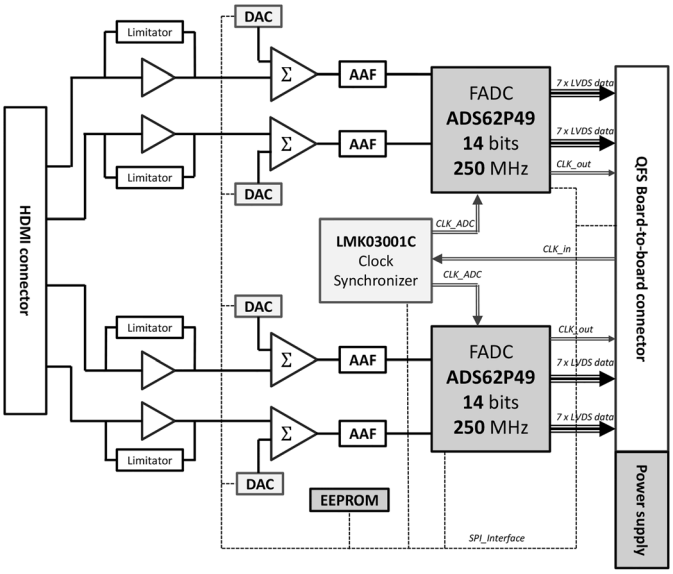

Fig. 4. FADC Mezzanine block diagram.

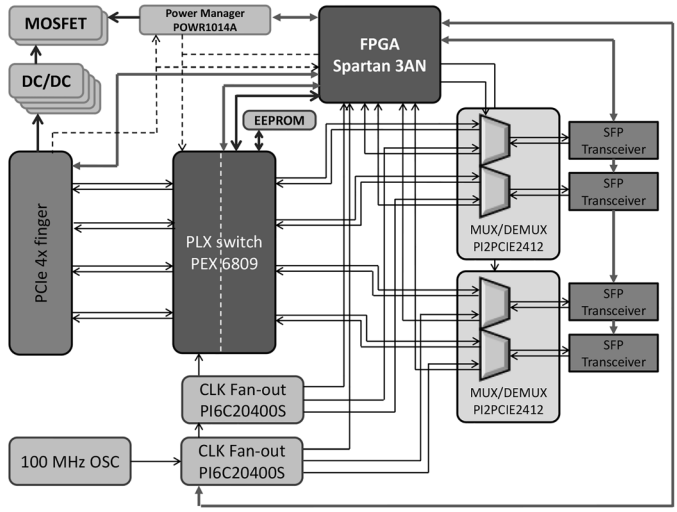

Fig. 5. LINCO2 board block diagram.

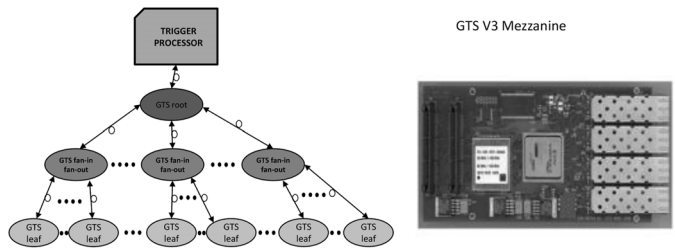

Fig. 6. GTS tree hierarchy and V3 Mezzanine picture.

and adding a degree of gain control. At the end of the analog stage, an 1st order passive antialiasing filter with a pole set at 100 MHz cuts off the undesired higher frequencies while preserving the signal rise-time.

The behaviour of the FADC Mezzanines has been evaluated both by measuring its intrinsic noise and calibrating it with a ^{60}Co source. Therefore, by applying the expression (1) over the intrinsic noise without any input added [13], the ENOB of the FADC Mezzanine can be obtained.

$$\sigma_e = \frac{R}{\sqrt{12}} \frac{1}{2^{ENOB}} \tag{1}$$

where σ_e is the experimental noise standard deviation in ADC counts and R is the dynamic range, also in ADC counts. Having obtained $\sigma_e = 1.4$, an ENOB of 11.7 is achieved.

Similarly, energy resolution measurements with radioisotopes were performed at GANIL (Grand Accélérateur d'Ions Lourds) in February of 2014, using ^{60}Co and ^{152}Eu sources with the setup of NUMEXO2 envisaged for EXOGAM and the data acquisition system from GANIL. An energy resolution of 2.3 keV@1.33 MeV demonstrated the suitability of the FADC Mezzanine in high-resolution gamma-spectroscopy applications as well.

The feasibility to implement digital PSA and TOF measurements with good timing measurements ($\sim$ 1 ns FWHM) has been commissioned at LNL (Laboratori Nazionali di Legnaro), using ^{60}Co and ^{252}Cf sources with the FADC Mezzanine. A timing resolution of 1.15 ns after applying spline interpolation and a NGD figure of merit $M = 1.3$ were obtained. These results which are comparable to the ones obtained in [6].

D. The LINCO2 Readout Boards

The LINCO2 boards are a set of adapter boards to translate the PCI express signals to/from the optical physical layer to legacy bus standards such as PCI (Peripheral Component Interconnect), cPCI, etc. Fig. 5 shows a picture of the LINCO2 block diagram.

LINCO2 boards have already been used for AGATA and for CMS (Compact Muon Solenoid) at CERN [11] in harsh environmental conditions. Each LINCO2 board contains 4 SFP optical connectors, a set of high-speed multiplexers which allow the selection either of clock or data signals, and a PLX high-speed switch PEX 8609 capable of working up to 20 Gbps which allows the interface between the optical fibres and the PCIe finger. A Spartan-3A is used to configure the high-speed blocks providing 3 different configurations: capability to transmit 4 clocks, 4 data lanes or 2 clocks and 2 data lanes.

E. The GTS System

An upgrade towards a fully-digital system requires the implementation of a system with the capability to synchronize all channels and to cope with the event validation/rejection. Inherited from AGATA [12], it is expected to be used in EXOGAM2 and NEDA, making possible different combinations of detector coupling.

GTS is based on a tree topology, and it contains three different types of firmware depending on the hierarchical solution: Firstly, the GTS leafs, at the bottommost position of the tree, placed inside the Virtex-5 in NUMEXO2. Out of the NUMEXO2, we find the Fan-in Fan-out and the Root units which are placed in GTS NIM (Nuclear Instrumentation Module) carriers, containing each, 4 GTS V3 Mezzanines. Fig. 6 shows the hierarchical GTS scheme and a picture of the V3 Mezzanine.

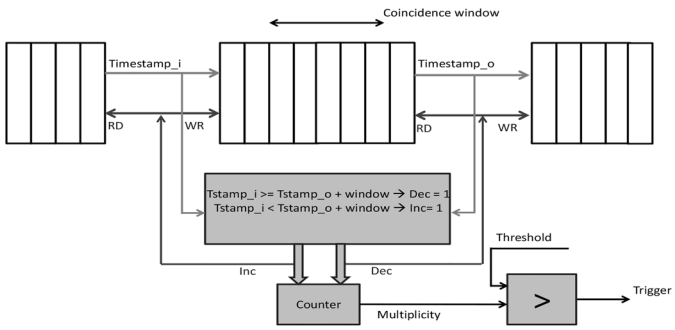

Fig. 7. Implementation of the multiplicity detection algorithm.

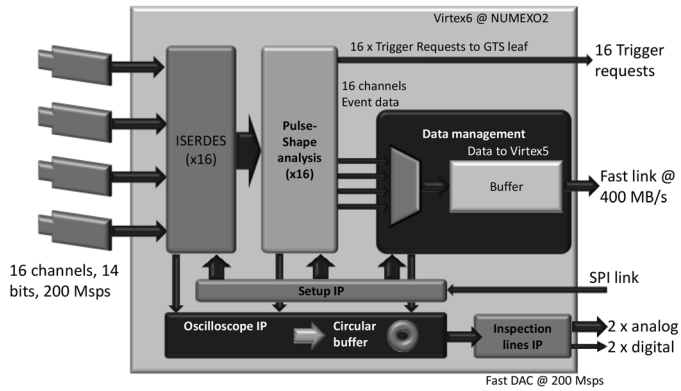

Fig. 8. Virtex-6 firmware blocks.

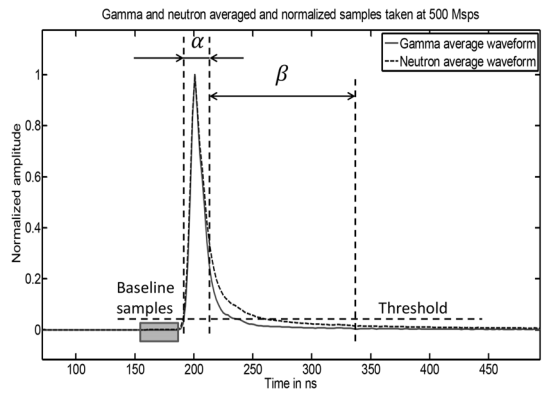

Fig. 9. Description of the charge-comparison method.

The GTS V3 Mezzanines include 4 optical links, 1 upstream and 3 downstream. Each upstream link from either the GTS leaf or a Fan-in Fan-out is connected to a downstream link from the GTS upper level. Finally, all nodes converge at the root node whose upstream link is connected to the trigger processor. The trigger processor is the element in the top of the GTS and it is in charge of coping with the event validation and rejection. NEDA, when using 21 NUMEXO2 boards (336 channels), requires a total number of 12 V3 Mezzanine units. NEDA Phase 1, with 45 channels only requires two V3 Mezzanines (1 Fan-in Fan-out and 1 root node) since only 3 NUMEXO2 boards would be used.

Each V3 Mezzanine contains a Virtex-4 to handle the optical transceivers. Two Mictor board-to-board connectors link the GTS Mezzanines to the carrier, where the slow-control commands are received via TCP/IP. The GTS carrier contains the Ethernet physical layer, power supply and a readout serial port connector, leaving all the complexity in the GTS Mezzanines.

The trigger processor consists of a commercial board Xpress GEN V5 200 connected to the upstream of the GTS V3 root Mezzanine. The algorithms to either validate or reject are different depending on the experimental context. As for the case of NEDA, which will be used for the detection of multiple neutron events, concerns the detection of multiple neutrons, proceeding to the detection of events within a time coincidence window. When performing this algorithm the trigger processor collects the timestamps of the incoming trigger requests. A buffer used as time coincidence window, compares the timestamps of the surrounding events, providing a validation for cases where the number of events within a coincidence window overcomes a certain threshold. Fig. 7 shows the algorithm.

F. Virtex-6 Firmware in NUMEXO2

The V6, explicitly the model V6-LX130T is the largest device in NUMEXO2, and carries out most of the pre-processing tasks such as deserialization, triggering algorithms, configuration and oscilloscope. Fig. 8 schematizes all points into a block diagram.

The first stage of data readout is performed by using a customized arrangement of ISERDES (Input SERialization and DESerialization) and IODELAY (Input/Ouput Delay) blocks, coping properly with the delay adjustment. ISERDES IP has been arranged to deliver at its output four 14-bit outputs, each containing the corresponding either even or odd samples from 2 FADC channels. The inputs of the ISERDES are the 7 LVDS (Low-Voltage Differential Signaling) even/odd multiplexed bit duplets plus the FADC output clock.

Following this, a PSA IP implements the charge-comparison method to reduce the trigger requests produced by gamma-rays. It delivers a trigger request to the GTS leaf if the PSA detects the incoming pulse as a neutron. The algorithm is based on the fact that neutrons and gamma rays excite the scintillator in different ways, producing different decay times which can be analyzed to obtain information regarding the particle type. Carrying this approach correctly entails the calculation of the integral across two regions: slow integral, which contains particle type information, and the fast integral, used to normalize the signal pulse area. Fig. 9 shows the time gates, denoted as α and β Commissioning tests have verified the suitability of the algorithm to perform this technique using time windows of $\alpha = 30$ ns and $\beta = 140$ ns.

The variable to perform the NGD histogram is called $\hat{\delta}$ defined as the ratio between the integrals after subtracting the baseline components (2).

$$\hat{\delta} = \frac{\hat{I}_s}{\hat{I}_f} = \frac{\sum_{n=\alpha+1}^{\beta+\alpha} v\,(n) - \bar{I}_b}{\sum_{n=1}^{\alpha} v\,(n) - \bar{I}_b} \tag{2}$$

where $v(n)$ makes reference to the input raw samples, $\hat{I}_s$ and $\hat{I}_f$ refer to the values of the slow and fast integrals after baseline subtraction and $\hat{I}_b$ is the averaged baseline value, which for our case taken along 32 samples. Then, the values $\hat{I}_s$ and $\hat{I}_f$ are

scaled and compared with a parameter $\hat{\delta}_t$ Hence, according to the aforementioned criterion:

$$T_{req} = 1 \; if \; \hat{I}_s \geq \hat{\delta}_t \hat{I}_f \; (neutron)$$
$$T_{req} = 0 \; if \; \hat{I}_s < \hat{\delta}_t \hat{I}_f \; (gamma) \qquad (3)$$

A trigger request T_{req} is sent to the GTS if the algorithm responds that the event was a neutron.

Pile-up cases are also detected during the PSA, producing two trigger requests and storing both waveforms. The time considered as pile-up is the time the PSA algorithm takes to perform the integrals. For the analysed case, with $\alpha = 30$ ns and $\beta = 140$ ns, a fixed term of 55 ns must be added. This is used to subtract the baseline and perform the comparison, leading to 225 ns. Each channel features a back-up unit in case of pile-up, calculating independently the integrals for both events.

The PSA algorithm has been tested using synthesized and normalized alternating gamma and neutron waveforms. The shortest value of has been found after optimization. Smaller values of β than 140 ns lead to worse NGD performance.

Raw data packets of 250 samples from the 16 channels are sent to the V5 if the PSA IP detects the event as a neutron. The data management unit stores temporally the events, aiming to organize the readout order in case of trigger requests which arrive closely in time and coincidences. A structure based on a parallel set of 3 FIFO (First-In First-Out) buffers for a single channel has been chosen in order to minimize the dead time, and to deal with the random nature of the events. Regarding the readout organization, the events are read in the same order as the trigger requests occurred. In case of coincidences, the channel with the lowest number is read first. Physically, the link between both FPGAs is implemented with 8 high-speed differential lanes. The protocol between devices is synchronous, using a 200 MHz DDR (Double Data Rate) clock to transmit the data towards the V5.

The Oscilloscope IP aims to monitor digital signals at different points of the processing of the 16 channels. The maximum frequency is 200 MHz and up to four probes can be simultaneously connected. The binary samples of each probe are continuously stored into a 32kBytes (or 16kWords) circular buffer and its content is frozen as soon as a trigger occurs. For each probe, the type of trigger and the time can be software-wise controlled.

Inspection lines are mainly envisaged to access internal signals, enhancing the testability of NUMEXO2. The front panel includes LEMO connectors which allow to drive out 2 analog (converted by means of high-speed DACs) and 2 digital signals in order to monitor them with an oscilloscope. The assortment of signals can be accessed by means of the internal multiplexers inside the V6 and the signal can be selected using the DAQ (Data AcQuisition) graphical user interface. Among the signals which can be selected, we find the raw-data input, the analog conversion of the frame which is sent to the V5, clocks, trigger signals and control lines.

Finally, a setup IP contains a set of registers used to configure the rest of the blocks within the Virtex-6, providing a flexible and dynamic firmware. Registers can be read and written using the software tool GECO (Ganil Electronic Control), working under the TCP/IP protocol via the Virtex-5. Some of the parameters the setup block takes control of are the IODELAY step value, PSA IP integration gates, among others.

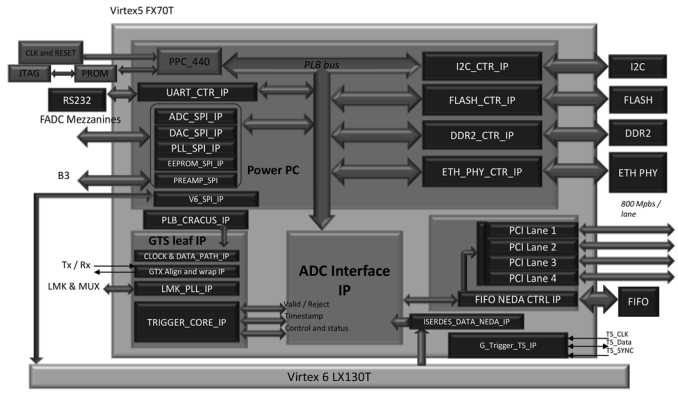

Fig. 10. Virtex-5 firmware blocks.

G. Virtex-5 Embedded software

Firmware and software on Virtex-5 are the link between the digitizer, the workstation and the GTS. The block diagram is shown in Fig. 10.

A big part of the tasks are implemented in the Virtex-5 PowerPC (PPC) 440 embedded processor with an embedded Linux OS. Inside the PPC most of the tasks related to communication driver management and register setup are implemented, such as the Ethernet Gigabit, configuration of the PCIe setup registers, the GTS leaf setup (performed through the PLB Cracus IP), register setup of the V6 and FADC Mezzanines, memory management of an external Flash (256 Mb) and DDR (1 Gb), and a serial port which allows to monitor the status of the Linux OS booting. Although Virtex-5 can be clocked from many sources, the PPC is the only device in the whole NUMEXO2 which must be clocked always from a local oscillator. TCP/IP is the main readout protocol used for EXOGAM2, although is not sufficient to deal with NEDA requirements. Nevertheless, during the preliminary test phases, the TCP/IP can provide a provisional solution for the readout, until the integration of the PCIe IP.

The ADC interface block carries out multiple functionalities on the other side of the Virtex-6. Mainly, the ADC IP connects the GTS leaf with the V6 and the readout via PCIe. After the GTS delivers a validation, the ADC sends the data attached with the timestamp to the PCIe readout.

Finally, the main readout is performed by the 4 PCIe Endpoint lanes, capable of running up to 10 Gbps, fulfilling NEDA specifications in terms of data throughput whereas 3.2 Gbps are required. Between the optical transceivers and the ADC interface, a 9 Mb FIFO is used to buffer the data between the ADC interface and the driver itself, aiming to fix the GTS and PCIe latencies. The data are received by the LINCO2 boards where the optical link is converted into a PCI standard to the legacy bus standards.

IV. Conclusions

A comprehensive digital front-end electronics system envisaged for the acquisition and pre-processing for NEDA detectors has been presented, starting from the next-to-the-detector

analog single-to-differential conversion stages up to the readout and GTS system. Even though some of the parts have been tested individually such as the FADC Mezzanines, LINCO2 boards, GTS tree and PSA performance, still a global test of the overall system has not been carried out yet. While the test of the overall system is expected for 2015, the first experiments with the new front-end electronics are envisaged for 2016.

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