A New Front-End High-Resolution Sampling Board for the New-Generation Electronics of EXOGAM2 and NEDA Detectors

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***Abstract*—This paper presents the final design and results of the FADC Mezzanine for the EXOGAM (EXOtic GAMma array spectrometer) and NEDA (Neutron Detector Array) detectors. The measurements performed include those of studying the effective number of bits, the energy resolution using HP-Ge detectors, as well as timing histograms and n/γ discrimination performance. Finally, the conclusion shows how a common digitizing device has been integrated in the experimental environment of two very different detectors which combine both low-noise acquisition and fast sampling rates. Not only the integration fulfilled the expected specifications on both systems, but it also showed how a study of synergy between detectors could lead to the reduction of resources and time by applying a common strategy.**

***Index Terms*—Acquisition in HP-Ge detectors, high-speed ADCs, low-noise electronics design.**

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I. Introduction

COMTEMPORARY studies in the field of nuclear structure of exotic nuclei has led physicists to build and use new high-resolution gamma spectrometers in order to achieve the levels of sensitivity in detection and energy resolution required by the challenging physics cases. Some examples of these new-generation detectors are: AGATA [1], EXOGAM [2](GANIL), NEDA [3], TRACE [4], etc.

Until few years ago, most of the detectors used analog front-end electronics to carry out the pre-processing tasks such as timing and energy processing to accurately measure those parameters. However, the physics demands have led to build up new detectors with larger number of channels, which can sustain higher counting rates. In addition, more complex algorithms are needed to track the gamma-rays in order to achieve higher efficiencies and better peak-to-background ratios. Consequently, the conventional front-end electronics were replaced by digital front-end systems.

Digital front-end systems have been successfully applied in several instruments [5]–[7], and are expected to be part of the instrument also in EXOGAM2, the EXOGAM electronics upgrade, and the new NEDA electronics. In this approach, high-speed A/D devices, fast communication optical links and reconfigurable logic devices are used at the front-end, improving the system robustness and flexibility. Our application has been designed in the framework of the NUMEXO2 (NUMériseur pour EXOGAM) digitizer [5], envisaged to be used for different detectors types, such as EXOGAM, a high-resolution gamma-ray spectrometer, and NEDA, a new-generation neutron detector used as an ancillary multiplicity filter. NUMEXO2 integrates the front-end pre-processing tasks such as energy and timing calculations, implemented in logic devices inside the motherboard. A set of 4 FADC (Fast Analog to Digital Converter) Mez-

zanines plugged onto the motherboard perform the sampling process [6].

From the detector requirements, it has been calculated that the noise contribution should be small enough that the ENOB (Effective Number of Bits) should be at least 11.3 in order to accomplish the desired energy resolution of 2.3 keV@1.33 MeV for EXOGAM. This specification is referred to the inner contact from each crystal, which is digitized with two dynamic ranges of 6 MeV and 20 MeV. For the 6 MeV channel, the energy threshold is set to 30 keV.

In case of NEDA, the PMTs are adjusted to obtain 1 V/MeVee (electron-equivalent). The main interest is focused on observing neutrons with kinetic energies up to 8 MeVee although the energy detection threshold is set at few tens of keVee. The FADC described in this paper provides sufficient number of channels, with better than 11.3 ENOBs required for our application. Furthermore, NEDA focuses also on NGD (Neutron-Gamma Discrimination) performance, requiring at least 200 Msps to deal with accurate timing measurements (Modamio, 2013) to perform TOF (Time of Flight) measurements and effective PSA (Pulse-Shape Analysis) methods [8]. Summarizing the specifications for both detectors, a resolution of 11.3 ENOB must be preserved when sampling at 200 Msps.

II. Design Issues

Each FADC Mezzanine contains four channels. After a thorough research for devices, the dual-channel ADC *ADS62P49*, with capability to sample up to 250 MHz and with 14-bits resolution (11.3-11.9 effective, depending on the specification type) was finally selected. Since one of the major noise contributions might come from a jitter-noised clock source, a jitter cleaner was added. According to the bandwidth of the type of signals involved, 100 MHz for NEDA while 35 MHz is sufficient for EXOGAM, a jitter contribution less than 1 ps [9] is required not to damage the ENOB. Therefore, after a device search, the *LMK03001C* was selected.

Another stage that plays a crucial role in terms of noise is the analog coupling stage preceding the ADC. Additionally, variable offsets using DACs (Digital-to-Analog Converter) are added in order to take full profit of the FADC dynamic range, allowing acquisition of both unipolar and bipolar signals. After a thorough study, the coupling is performed by means of AD8139 FDA (Fully-Differential Amplifier). At this stage, also the gain control is carried out to select either 6 or 20 MeV energy ranges. Fig. 1 depicts the FADC Mezzanine block diagram.

The aforementioned energy ranges can be translated at the level of the Mezzanine as voltage-to-voltage gains, which are, 1 and 0.25 respectively. Due to stability conditions, the amplifier must work slightly over unity gains, as lower gains make it unstable. Moreover, the noise performance conditions are optimal for unity gain, worsening for higher gains. Due to the noise constraints and stability issues, the design strategy consisted of using two AD8139-based stages work under unity gain. The attenuation factor of 0.25 can be then achieved by adding a T-divider in between both stages so that the division ratio and the impedance seen backwards from the amplifier can be designed

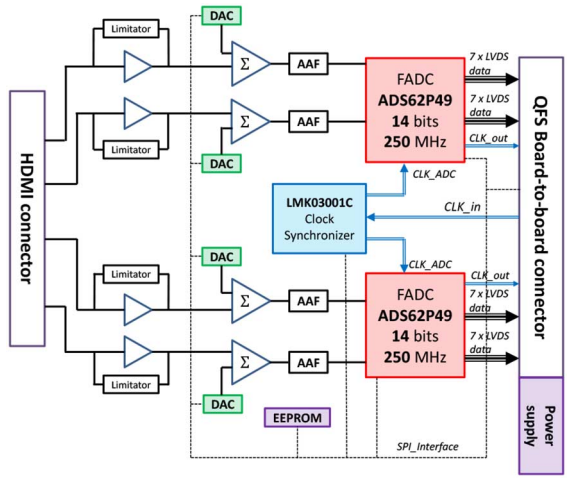

Fig. 1. FADC Mezzanine block diagram.

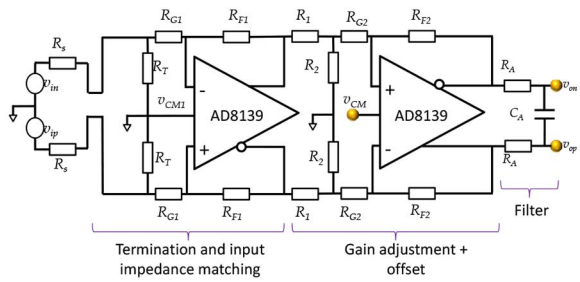

Fig. 2. High-speed analog driver schematic diagram.

independently. Based on the schema from Fig. 2 the high-speed analog driver can be designed by from the following expressions (1), (2) and (3).

$$Gain = \frac{R_{F2}}{R_{G2}} \frac{1}{R_1} \left(\frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{G2}}} \right) \tag{1}$$

$$R_{F2} = R_{G2} + R_1 || R_2 \tag{2}$$

$$R_T || R_{G1} = 50\ \Omega \tag{3}$$

where R_{Fi}, R_{Gi} refer to the feedback and input resistors of each i-th analog AD8139 stagerespectively, R_1 and R_2 are the T-divider resistors, and R_T is the input terminator. Equation (2) must be applied in order to make the AD8139 work as a unity-gain amplifier while 1) is obtained after applying Kirchoff's laws to the T-divider and the second stage input nodes. Finally, 3) is used to match the terminator impedance with the cable impedance provided that the cable has 100Ω differential impedance. According to the amplifier datasheet, for optimal performance, R_{Gi} and R_{Fi} should be set to 200Ω, fact which leads the choice of $R_T = 66\Omega$, $R_{G1} = R_{F1} = R_{F2} = 200\ \Omega$, $R_{G2} = 100\ \Omega$. R_1 and R_2 have different values depending on the gain configuration, which are $R_1 = 400\ \Omega$, $R_2 = 133\ \Omega$ when using the gain configuration at 0.25, and $R_1 = 100\ \Omega$ and R_2 open in case of unity gain.

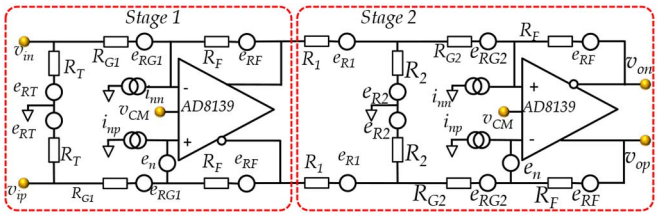

Fig. 3. Analog stage noise model.

A lower-speed analog driver is needed for driving the offset voltages from the DAC to the high-speed analog stage using a side-summing branch. The analog stage contains an antialiasing filter placed before the FADC device based on a single-pole RC filter with 100 MHz cut-off frequency. The total RMS noise can be obtained by means of the fully-differential amplifiers noise models. Including the contributions from the resistors and the amplifier, the circuital noise model can be described as in Fig. 3.

The AD8139 involve intrinsic spectral voltage and current noise densities of $2.25\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $2.2\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$ respectively. The equations have been developed by referring the voltage noise densities at the output of each sub-stage. Afterwards, taking the gain of each sub-stage and the contribution of each stage into account separately, both terms can be gathered using Friis' formula. Expression 4) shows the total noise contributions from the first sub-stage. The calculations do not assume the frequency behaviour of each contribution to vary all sources are assumed to be Gaussian.

$$e_{o\_s1}^2 = e_n^2\left(1+\frac{R_F}{R_{G1}}\right)^2 + i_{nn}^2R_F^2 + i_{np}^2R_F^2 + 8kTR_F + 8kTR_{G1}\left(\frac{R_F}{R_{G1}}\right)^2 + 8kTR_T\left(\frac{R_F}{R_{G1}}\right)^2 \tag{4}$$

the second sub-stage, including also the voltage divider

$$e_{o\_s2}^2 = e_n^2\left(1+\frac{R_F}{R_{eq}}\right)^2 + i_{nn}^2R_F^2 + i_{np}^2R_F^2 + 8kTR_F + 8kTR_{G2}\left(\frac{R_F}{R_{eq}}\right)^2 + 8kTR_1\left(\frac{R_F}{R_{eq}}\right)^2\left(\frac{R_2||R_{G2}}{R_2||R_{G2}+R_1}\right)^2 + 8kTR_2\left(\frac{R_F}{R_{eq}}\right)^2\left(\frac{R_1||R_{G2}}{R_1||R_{G2}+R_2}\right)^2 \tag{5}$$

where $R_{eq} = R_{G2} + R_1||R_2$. For the resistor values used in the design, e_{o_s1} and e_{o_s2} are $5.83\ \mathrm{nV}/\sqrt{Hz}$ and $6\ \mathrm{nV}/\sqrt{Hz}$ respectively. When square-summing both, assuming that the second amplifier is working under unity gain, the total spectral noise density, e_{o_s} rises to $8.36\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. This spectral density must be integrated over the bandwidth to obtain the total RMS noise. In case of having a first-order antialiasing filter, as is the case here, the equivalent bandwidth of the filter is $B_{eq} \cong 1.57f_c$, where f_c is the cut-off frequency. For cut-off frequencies of 30 MHz and 100 MHz, the total RMS noise is 57.4 μV and 104.8 μV, less than the ADC LSB voltage value of 122 μV.

TABLE I
CABLE TESTS AND RESULTS

Element	BW	Crosstalk	EMI
MDSM	--	43.8 mV	--
HDMI	70 MHz	4.18 mV	1.07 V
HDMI 1.4 Infinite	120 MHz	3.82 mV	356 mV
PoCL-Lite	35 MHz	8.02 mV	6.25 V

Another important point is the connection between the Mezzanine and the front-end electronics. Quality tests such as bandwidth, crosstalk and EMI were applied to the cables *MDSM*, *HDMI* standard, *HDMI* version 1.4 *'Infinite'* and the *PoCL-Lite* cable. To clarify the numbers obtained in Table I, the bandwidth tests were carried out including the front-end board, meaning that the numbers shown are referred to the bandwidth of the overall chain in front of the FADC Mezzanine. For the crosstalk tests, square waveforms with 1 V amplitude and 2.5 ns rising and falling edges were used. As the cable uses differential pairs, the crosstalk measured is also shown as the difference peak-to-peak of the crosstalk obtained in each conductor. EMI tests were performed by covering the far-end side of the HDMI cable with a foil paper, through which 1 kV low-current pulses were injected with a frequency of 50 Hz.

The interface of the FADC Mezzanine to the motherboard is achieved using two board-to-board connectors, connecting slow-control signals, high-speed data, clocks and power nets.

Regarding the power supply design, as the FADC Mezzanine requires several voltages for analog, mixed and digital devices, the main devices such as the FADC and PLL are supplied by their own LDOs (Low Drop-Out regulator) independently. This strategy was not followed only to decrease the temperature in the LDOs, but also to isolate the noise produced by the jitter-clock cleaner influence, into the A/D converters.

Finally, aiming to simplify the slow-control firmware and hardware it has been sought that all programmable chips in the FADC Mezzanine would have the same slow-control protocol. Therefore, chips such as the FADC device, PLL, DACs and EEPROM all make use of the SPI protocol. Regarding the board layout, 12 layers have been used to properly isolate the high-speed digital from analog traces, properly guiding the return current paths, minimizing the influence on the most sensitive traces. The Mezzanine size is 98.5 × 42 mm fitting with NUMEXO2 specifications.

III. DESIGN OF A TESTBENCH PLATFORM

A testbench platform was developed to verify the FADC Mezzanine performance, on one hand including standard A/D conversion parameters such as SINAD, ENOB, THD, and, on the other hand, parameters linked to acquisition qualities specific for the field of nuclear physics, such as the energy resolution, timing resolution and neutron-gamma discrimination performance.

The Mezzanine is tested using a ML605 Evaluation Module (which contains a Virtex-6 FPGA), to set up the FADC Mezzanine via SPI, and also buffer and read out the data using the serial port. The interface to the ML605 is achieved by means of an intermediate board while the connection to the waveform generator is carried out using a front-end single-ended conversion board, which also makes use of the *AD8139*. The interaction with the user is carried out on the software part, which is performed with a GUI based on LabView. The GUI allows sending commands to the FADC Mezzanine, monitoring and analysing data.

IV. Results

The following measurements were applied to the FADC Mezzanine to verify its behavior:

A. Intrinsic Electronic Resolution

The noise performance was initially evaluated by measuring the intrinsic noise from the FADC Mezzanine itself. During this process, not only the noise from the FADC device is caught, but also from the analog stages in front. Expression (4) is used to calculate the ENOB from the noise standard deviation (L. Bardelli, 2006) where σ_e is the standard deviation measured in ADC counts.

$$\sigma_e = \frac{R}{\sqrt{12}} \frac{1}{2^{ENOB}} \tag{6}$$

The measurements have been performed at 100, 200 and 250 Msps, and bandwidths of 50 and 100 MHz. One of the most interesting observations is to study the standard deviation evolution as a function of the ADC code, exploring the resolution across the whole range.

Fig. 4 shows how the resolution changes with the sampling frequency, obtaining a flattened response of σ_e with 1.3-1.5 at 100 Msps, 1.4 - 2 at 200 Msps and 1.4 - 3.5 at 250 Msps. The effect of the peaks at 250 Msps has been well studied, being caused by crosstalk converted into noise due to influence of digital lines on analog traces. The effect appeared in former Mezzanine versions at 200 Msps, with variations of σ_e between 1.4 and 3.5 at 200 Msps. A layout improvement has led to a drastic reduction of the peak at 200 Msps, still being present at 250 Msps. However, 250 Msps is not expected to be used in experimental environment due to an incompatibility with the Global Trigger and Synchronization (GTS) system (Bellato, 2013)[11].

B. Energy Resolution Measurements with HP-Ge Detectors

Energy resolution measurements were carried out at GANIL in February 2014 using a HP-Ge EXOGAM crystal and the radioisotopes ^{60}Co and ^{152}Eu. To carry out this test, the NUMEXO2 firmware and DAQ was used instead of the aforementioned testbench platform due to the requirement of a hardware-wise-implemented Moving Window Deconvolution (MWD) [12](Georgiev, 1994) algorithm to extract the energy with higher resolution. The experimental setup involved the whole electronic chain, using a ^{60}Co source to measure the

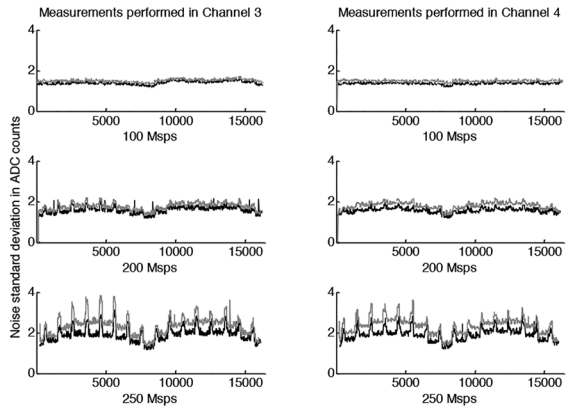

Fig. 4. Resolution performance for Channels 3 and 4 at different sampling frequencies (100, 200 and 250 Msps), and bandwidths. Plots in black describe the measurements with 50 MHz bandwidth while the grey line stands for 100 MHz bandwidth.

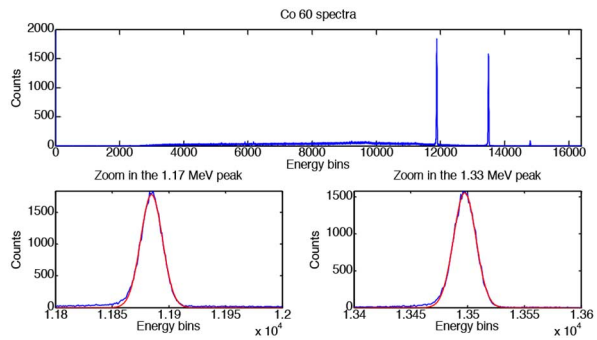

Fig. 5. Energy resolution measurements using a ^{60}Co and a HP-Ge detector from EXOGAM.

TABLE II
^{152}Eu Energy Peaks and Their Resolution

Energy	FWHM (keV)	Energy	FWHM (keV)
44	1.8	778	2.13
121	1.69	1112	2.29
344	1.77	1408	2.31

energy resolution at 1.33 MeV and the ^{152}Eu to calibrate the system in a wider range of energies.

Obtaining the finest energy resolution depends, not only on the noise performance, but also on the overall gain. The electronic chain contains two instances where the gain can be changed, the FADC Mezzanine and the trapezoidal filter. Optimal results have been obtained with a unity gain for the FADC Mezzanine combined with the MWD parameters K $= 18.6$ μs (slope) and M $= 2$ μs (flat-top). Using the energy peaks from ^{60}Co, the energy resolution can be extracted using the amount of energy per LSB. Fig. 5 shows the spectrum obtained for the ^{60}Co source.

By applying a Gaussian fitting to both peaks, it was verified that the 2.3 keV@1.33 MeV was obtained according to the specifications. Similarly the spectrum for the ^{152}Eu source is used to calibrate in a wider range of energies and to obtain the low-energy detection threshold, a critical issue for the digital signal processing. Fig. 6 shows the energy spectra taken with the ^{152}Eu

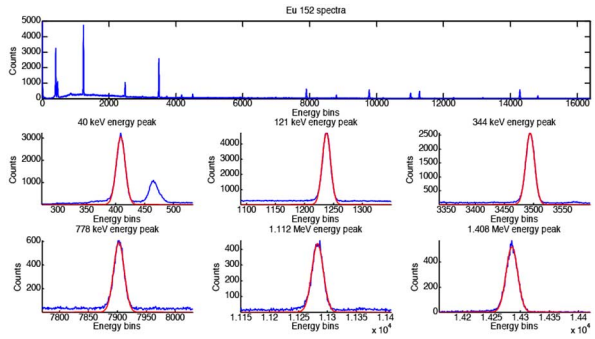

Fig. 6. Energy resolution measurements using a ^{152}Eu and a HP-Ge detector from EXOGAM.

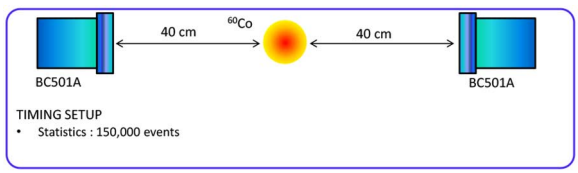

Fig. 7. Physical set-up for timing resolution measurements.

source ($<$ 100 Hz), and a zoom in all the peaks after performing a Gaussian fitting.

where the energy peaks and their resolution are summarized in Table II.

Furthermore, the measurement with ^{152}Eu allows visualization of low-energy X-rays (44 keV), coping with the lowest threshold setup, which, in case of EXOGAM, is set to 30 keV according to the specifications.

C. NGD Performance

Timing resolution and PSA performance are of paramount importance to perform NGD in neutron detectors, being one of the main qualification parameters taking part in the verification of NEDA electronics. Unlike the energy resolution tests with HP-Ge detectors, performed with the NUMEXO2 board, FADC Mezzanine tests with NEDA detectors were carried out using the testbench mentioned in Section III, since part of the firmware blocks were not yet developed. Therefore, NIM modules used for the analog processing in the Neutron Wall [13] such as CFD (Constant Fraction Discriminator), coincidence and Fan-in Fan-out modules, were used to deliver the trigger signal to the FPGA in order to start the acquisition. The digitized data is stored in a disk for further processing applying off-line algorithms. The setup was established at LNL (Laboratori Nazionali di Legnaro) in February 2013, using the FADC Mezzanine at 200 Msps and 100 MHz bandwidth.

In case of timing measurements, two BC501-A detectors were placed 40 cm away from the ^{60}Co source forming 180°, as it is depicted in Fig. 7.

The trigger signal is generated using a coincidence after the both signals from both BC501-A detectors pass by a CFD. When a trigger is generated, it starts the pulse buffering in the FPGA with a total event length of 2048 per event. Fig. 8 shows how the NIM modules have been connected in order to provide the trigger signal to the FPGA.

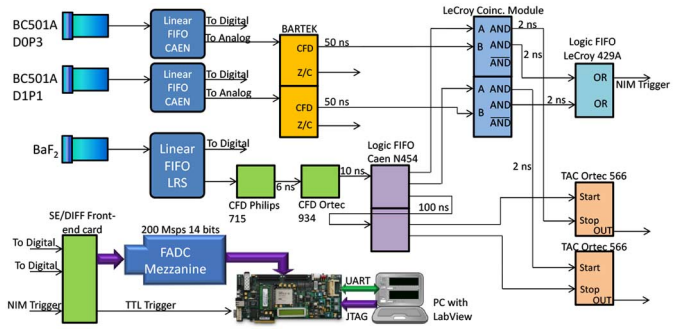

Fig. 8. Electronic set-up for timing resolution and PSA performance measurements.

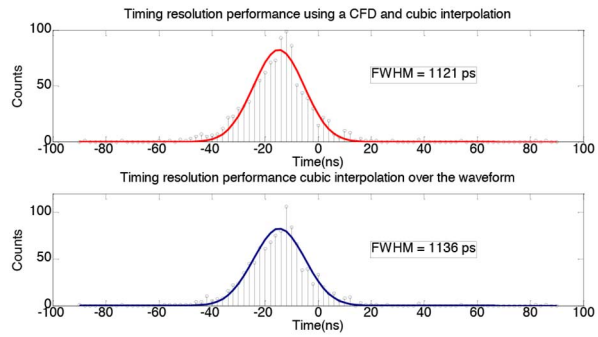

Fig. 9. Timing resolution histograms. Left) after applying cubic spline to a dCFD signal. Right) after applying a cubic spline to the original signal.

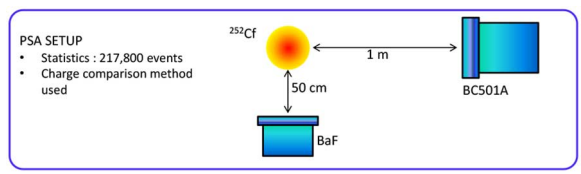

Fig. 10. Physical set-up for PSA performance measurements.

For timing resolution, measurements, the algorithms which have been compared consist of a set of cubic spline interpolation algorithms [7](Modamio, 2013) applied both to the original signal and to a digital CFD. Using the interpolated waveform, a threshold is applied to both signals, hence calculating the time difference, the value which is plotted in the histogram. The timing resolution is extracted after performing a Gaussian fit over the histogram with at least 10,000 events. The results show resolution of 1.121 ns FWHM for the interpolated dCFD and 1.136 ns FWHM if using the interpolation on the original signal. From the results it can be concluded that the performance obtained with this FADC Mezzanine is similar for both algorithms, both cases being applicable for NEDA detector, which requires a minimal resolution of 1.5 ns FWHM. Fig. 9 shows the timing histograms for both algorithms and the resolution obtained after applying a Gaussian fitting function.

On the other hand, for PSA performance measurements, only one detector was placed 1 m away from the ^{252}Cf source. The algorithm used is the charge-comparison method [8], which compares the charge integrated across different waveform regions, i.e. slow integral, which contains particle type information, and the fast integral, used to normalize the signal

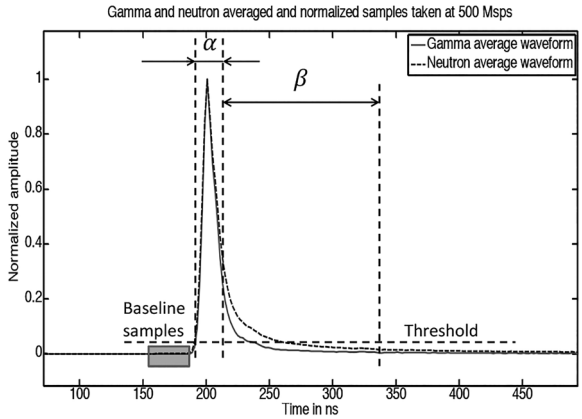

Fig. 11. Description of the charge-comparison method.

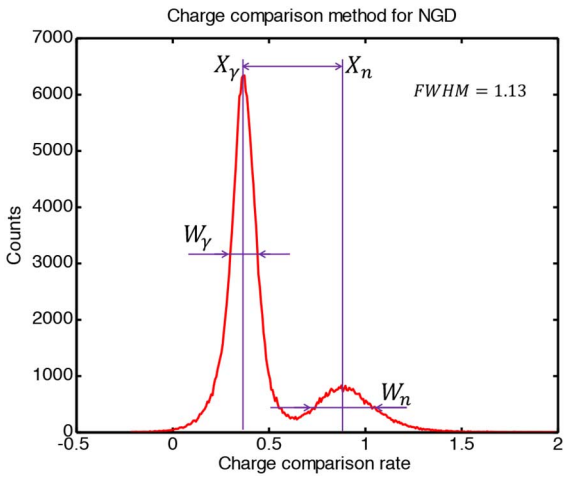

Fig. 12. Charge-comparison histogram obtained with the FADC Mezzanine.

pulse area. Fig. 10 shows the physical set-up used to obtain the samples from the ^{252}Cf source using $> 200,000$ events, and Fig. 11 shows a graphical description of the charge-comparison method. The time gates at which the integrals are calculated have been denoted as α (fast) and β (slow).

The observable variable to perform the NGD histogram is called $\hat{\delta}$, defined as the ratio between the integrals after subtracting the baseline contribution $\overline{I_b}$.

$$\hat{\delta} = \frac{Slow\ integral}{Fast\ integral} = \frac{\sum_{n=\alpha+1}^{\beta+\alpha} v\,(n) - \overline{I_b}}{\sum_{n=1}^{\alpha} v\,(n) - \overline{I_b}} \tag{7}$$

where $v(n)$ constitutes the reference for the input raw samples and $\overline{I_b}$ is the averaged baseline value, for our case taken along 32 samples. A histogram is generated using the aforementioned value $\hat{\delta}$, where two lobes can be distinguished. The figure of merit M, defined as:

$$M = \frac{|X_\gamma - X_n|}{W_\gamma + W_n} \tag{8}$$

is then used to obtain the quality the discrimination, where X_n and X_γ are the neutron and gamma peak positions on the histogram, and, W_n, W_γ are their FWHMs. Fig. 12 shows an example of a histogram obtained with $\alpha = 25$ ns and $\beta = 500$ ns, while in Fig. 13 it is presented a plot which compares the figure of merit given for several values of α and. The histogram β over which the measurements were taken is shown in Fig. 12, where a value of $M = 1.13$ was obtained.

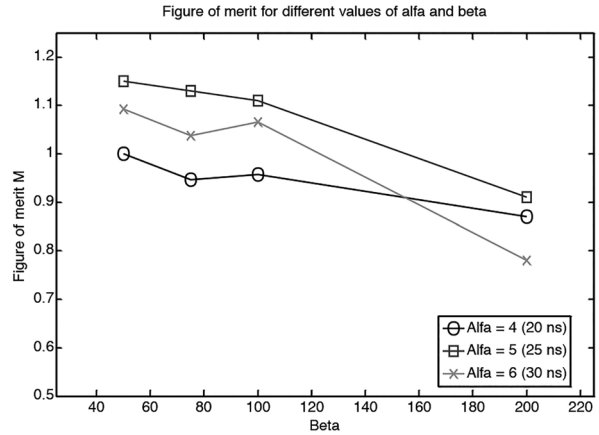

Fig. 13. Comparison of the figure-of-merit performance for several values of α and β.

V. Conclusions

The results obtained have reported an excellent behaviour in terms of noise, a fact which motivated the usage of the FADC Mezzanine in the experimental environment with the detectors, obtaining also, a performance fulfilling the specifications from both EXOGAM and NEDA. Regarding the usage in EXOGAM, the resolution of 2.3 keV@1.33 MeV confirms that, even though the resolution is slightly lower than in pure analog systems (2.16 keV@1.33 MeV), the improvement of the overall system bandwidth, capabilities, flexibility and counting rate verifies the suitability of this design in an environment for high-resolution gamma-spectroscopy.

On the other hand, regarding the integration of the sampling board for NEDA, it has been demonstrated that by using a digital sampling system at 200 Msps, a timing resolution close to 1.12 ns FWHM can be obtained, suitable for the application along with a figure of merit $M = 1.13$. This figure of merit verifies that the digital techniques of the PSA analysis can later on be applied to enhance the NGD performance using this sampling board.

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