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Multi agent system based adaptive numerical relay design and development, Part II: Hardware

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ABSTRACT

Integrating multiple feeders and power sources into the electrical grid necessitates more robust protection systems. Existing numerical relays require manual reconfiguration of each relay for any network or protection setting modifications and are unable to effectively coordinate fault clearance when bidirectional energy flow is present. One of the major contributions of this work involves integrating adaptive protection features that enable automatic updating of protection configurations across all relays for any network configuration change, eliminating the need for manual adjustments and enhancing fault clearance coordination. This article, which is Part II of the series of articles derived from the research work conducted to develop a multi-agent system (MAS) based adaptive protection relay, delves into the hardware design of an adaptive protection relay. The complementary Part I article has covered the firmware aspect of the developed relay by providing a detailed discussion of the implemented adaptive algorithms. The hardware design encompasses various crucial modules, including the power supply, processor, digital input and output, analog input, and the Human–Machine Interface (HMI) modules. STM32MP157 microprocessor is utilized as the central processor handling all the firmware of the adaptive protection relay. Various adaptive protection coordination tests have been successfully conducted on the developed hardware modules.

1. Introduction

Power system protection is an invaluable part of modern electrical grids. Various multi-functional protection relays nowadays have advanced protection and communication features. With the integration of multiple feeders and sources, there arises a need for a more advanced protection scheme that takes into account the direction of energy flow as well as the change in the network configuration because of the addition or removal of sources or loads.

Utilizing the TMS320F2812 DSP, [1] attempts to develop an overcurrent relay and provides MATLAB simulation and hardware implementation results. In [2], the performance of a MATLAB-SIMULINK based design of an overcurrent relay is compared with IEC standard equation and ETAP simulation results. The design and implementation of a microcontroller-based multifunctional relay for equipment protection against over-current, over-voltage, and under-voltage, which is also validated through simulations and hardware prototypes, is presented in [3]. Similarly, [4] introduces a digital multi-function protection relay that incorporates diverse protection schemes, including overcurrent, overvoltage, undervoltage, over-frequency, and under-frequency.

In [5], a novel single-phase overcurrent protection relay that utilizes an Arduino NANO for design and implementation is introduced, offering enhanced operating flexibility and responsiveness. The research works indicated in [6,7] introduce the development of multi-functional numerical relays with advanced processors. In [8], a comprehensive numerical relay development environment is introduced, comprising a computer-based hardware-in-the-loop test bench setup. An overcurrent relay protection technique utilizing field-programmable analog arrays (FPAAs), highlighting the advantages of a simple and highly efficient design, is presented in [9].

The study in [10] introduces a novel protection relay based on ARM and DSP, utilizing the ARM processor's network communication features along with the efficient capabilities of DSP to accomplish feeder protection functions. Meanwhile, in [11,12], an FPGA-based multi-functional protection relay has been implemented, showcasing its wide-ranging capabilities. Additionally, [13] presents the design and implementation of two protection relays capable of handling fault conditions, such as overcurrent, by utilizing both FPGA and microcontroller platforms.

As indicated in [14–17], adaptive protection has become the leading and progressive method that can guarantee efficient protection with

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the inclusion of multiple sources and feeders into the electrical grid. The protection method discussed in [18] deals with multi-categorical ways of handling power system faults. Meanwhile, the study in [19] discusses using multi-agent systems to improve the electrical grid's stability during temporary disturbances. A new way of analyzing and managing faults in smart distribution networks using a combination of two relay systems and configuration agents is suggested in [20], while [21,22] explore the use of multi-agent system architectures for smart distribution networks. In [23], a multi-agent system that delivers a comprehensive solution for coordinating and protecting power grids is proposed, while this approach is demonstrated in [24].

Modern protection relays cannot efficiently coordinate fault detection and isolation in the presence of a bidirectional flow of energy. Manual reconfiguration of each relay is also necessary for any network or protection setting modifications. This work's primary contributions include incorporating adaptive protection coordination features that facilitate fault clearance coordination and automatically updating protection settings in all relays. The protection schemes suggested in [23] have been utilized to develop the adaptive protection relay. There is also a lack of significant resources in the literature that thoroughly analyze developing a fully functional adaptive protection relay based on multi-agent systems to resolve these predicaments. The complementary Part I article has incorporated the detailed software features of the developed adaptive protection relay. However, this Part II article delves into the overall design approach and the hardware modules used in the development process. Section 2 provides detailed descriptions of the hardware structures of the developed adaptive protection relay based on the multi-agent system. A thorough analysis of the schematic and PCB designs of the hardware modules, along with various practical test results, is presented in Section 3.

2. Hardware structure of the adaptive protection relay

Modern protection relays comprise several modules that interact with each other to protect the electrical grid effectively. Fig. 1 depicts the basic hardware boards and the primary components of each board for the developed adaptive protection relay. These boards include a power supply and digital I/O board, analog input board, processor board, human–machine interface (HMI) board, and current/voltage transformer (CT/VT) board. In order to achieve a compact design, the power supply module, digital input module, and digital output module have been placed on the same board. Signals and data exchange between the various boards is accomplished via interconnects. Detailed descriptions of these modules are provided in the subsequent sections.

2.1. Power supply module

The power supply module ensures that components operate by providing the required voltage and current inputs. This work utilizes the switch mode power supply (SMPS) because of its stability and high efficiency. An SMPS is an electronic circuit that utilizes switching devices to convert power by rapidly turning them on and off at high frequencies. It can provide regulated and reliable outputs, regardless of fluctuations in the input supply voltage, while also being of compact size. A basic isolated AC to DC switched-mode power supply comprises several components, including an input rectification, a start-up circuit, switching devices, an SMPS transformer, an output rectification, and a feedback control unit.

Various isolated SMPS topologies, such as flyback and push-pull, with distinctive characteristics and operating modes, dictate how input power is transferred to the output. For low-power applications, the flyback converter is a widely used SMPS circuit known for its simplicity and low component count. The basic structure of the flyback SMPS is depicted in Fig. 2. Its core component is the flyback transformer which provides isolation and prevents simultaneous current flow in the primary and secondary windings via phase reversal as indicated in

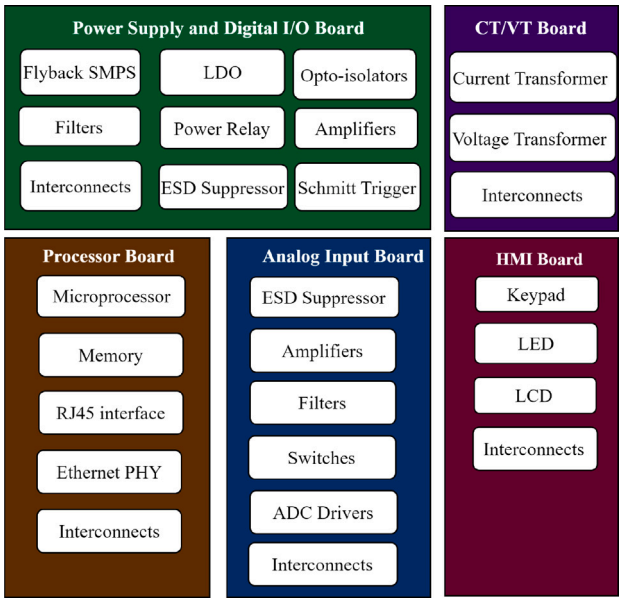

Fig. 1. Primary components of the hardware modules.

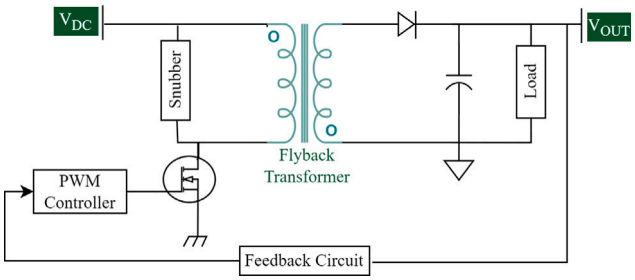

Fig. 2. A basic functional structure of an isolated flyback SMPS.

Fig. 2. Adding extra windings to the transformer can generate multiple output voltages, while regulation can be based on single or multiple outputs.

This work utilizes a single-output SMPS due to its simplicity and reliable feedback regulation. Low dropout voltage regulators (LDO) have been employed to obtain specified voltage levels (+12 V, -12 V, 5 V, and 3.3 V) required for components of the protection relay from the 15 V output voltage. Fig. 3 illustrates the overall functional blocks of the developed power supply module with multiple outputs. The reference designs and guidelines provided in [25–27], along with other application notes, have been analyzed prior to developing the power supply module.

In order to meet regulatory requirements, ensure reliable functionality, and safeguard against potential harm from overload, short circuits, or voltage fluctuations caused by lightning strikes or electrostatic discharges, the designed power supply incorporates protective components such as fuses and metal-oxide varistors (MOV). To mitigate the potential transmission of common mode noise, an Electromagnetic Interference (EMI) filter is placed prior to rectification. The bridge rectifier and filtering unit generate a DC voltage output. A snubber circuit such as RCD or TVS is imperative to protect the MOSFET from avalanche breakdown. In contrast to the RCD snubber, which exhibits variations in snubber voltage with changes in drain current, the TVS maintains a consistent snubber voltage irrespective of the drain current fluctuations. The implementation of TVS in this research also aims to achieve reduced power consumption during light load conditions. The start-up circuit provides an initial charging current for the start-up capacitor required for the operation of the PWM controller. UC3845 PWM

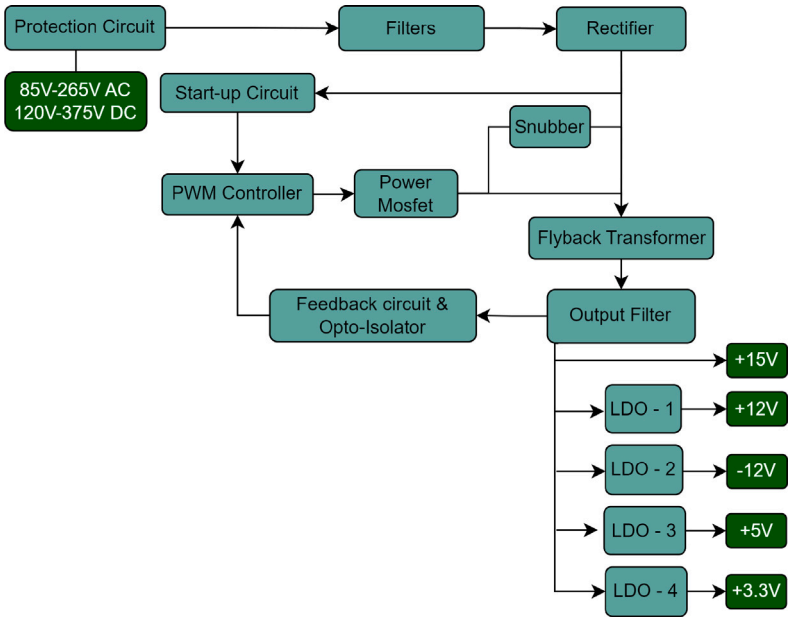

Fig. 3. Functional blocks for the overall power supply module.

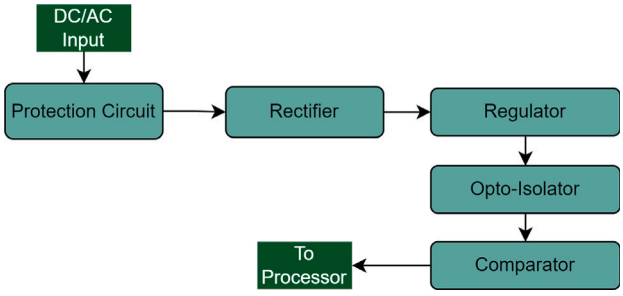

Fig. 4. Functional blocks of the digital input module.

controller [28] is employed as a switching IC for generating pulses that determine the output voltage. A TL431 three-terminal adjustable shunt regulator [29] is utilized for secondary side regulation in the developed flyback SMPS. Opto-couplers have been used to isolate the secondary side of the SMPS from the primary side.

2.2. Digital input module

A digital input module is necessary to acquire status signals from switches, circuit breakers, or other relays. Its functional blocks are provided in Fig. 4. The digital input module developed in this work can accept AC and DC inputs and provide the corresponding digital equivalent to the processor. A metal oxide varistor (MOV) is employed to protect against over-voltage transients. The rectification stage is necessary to supply DC voltage input to the linear regulator. LR8 [30] linear regulator-based circuit, which has a wide input range (13.2 V to 450 V) is utilized to produce a stable voltage that serves as an input to the optocoupler. The use of optocouplers is necessary to provide optical isolation for the input channel of the microprocessor. SN74AC14 [31] hex Schmitt-trigger inverter is used as a comparator to generate two digital outputs that correspond to the status of the switches or circuit breakers (Open or Closed). This output is then supplied to the micro-processor for further analysis. In this work, four digital input units have been implemented.

2.3. Digital output module

A digital output module is required to send digital signals to circuit breakers or other relays. The basic functional block of the developed digital output module is illustrated in Fig. 5. The isolation and control circuit contains an optocoupler for isolation and a transistor to control the operation of the power relay. JQX-115F [32] high power relay, which has 16 A switching capability, is utilized to send commands to circuit breakers or other relays. In this work, four digital output units have been implemented.

2.4. Current and voltage transformer module

The current and voltage transformer module is designed to isolate and step down the incoming current and voltage signals. ZMCT123 current transformer [33], which can operate for an input current range of 0 to 100 A, is utilized in this work. Equipped with a turns ratio of 1:2000, ZMCT123 can significantly reduce a 5 A input current to a safe 2.5 mA value to be processed by the analog input circuitry. The sampling resistor depicted in Fig. 6 is essential to obtain the voltage level corresponding to the input current using Eq. (1). The value of the sampling resistor utilized in this work is 20 Ω. Where: V_{out} = Sampling voltage I_{in} = Input current R_{samp} = Sampling resistor

$$V_{out} = \frac{I_{in} * R_{samp}}{2000} \tag{1}$$

ZMPT101B current-type voltage transformer [34] is utilized in this work. It has a turns ratio of 1000:1000 and a rated input and output current of 2 mA. Fig. 7 depicts a basic ZMPT101B-based circuit. The resistor R_{lim} has a very high value and limits the current going into the voltage transformer. The sampling resistor R_{samp} is introduced to obtain the output voltage using Eq. (2). The values of the limiting and sampling resistors employed in this work are 820 kΩ and 100 Ω, respectively. This transformer can accept input voltages in the range of 0–1000 V. In this work, four current and four voltage transformer units have been successfully implemented.

$$V_{out} = \frac{V_{in} * R_{samp}}{R_{lim}} \tag{2}$$

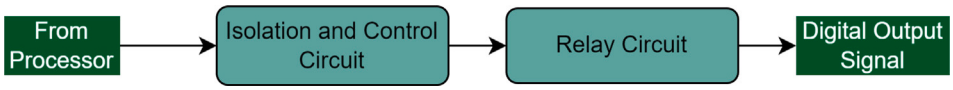

Fig. 5. Functional blocks of the digital output module.

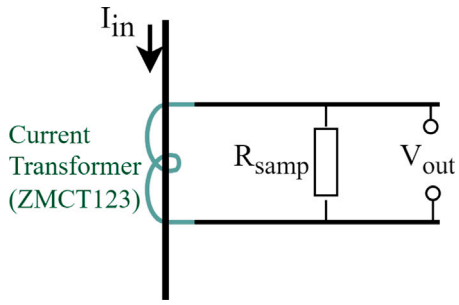

Fig. 6. Sampling circuit for ZMCT123 current transformer.

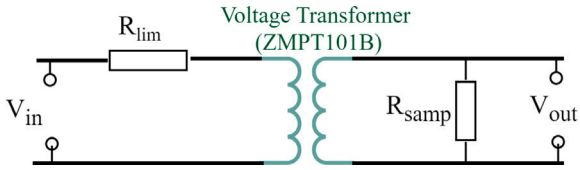

Fig. 7. Sampling circuit for ZMPT101B voltage transformer.

Where:

V_{out} = Output voltage

V_{in} = Input voltage

R_{lim} = Limiting resistor

R_{samp} = Sampling resistor

2.5. Analog input module

The analog input module is designed to filter and optimize incoming signals from the transformer module. The overall functional block diagram for the developed analog input module is provided in Fig. 8. The reference designs and recommendations provided in [35], along with other application notes, have been analyzed prior to developing the analog input module. Signal conditioning is essential before introducing signals from CTs and VTs to sensitive electronic circuits. It is crucial to include protective devices capable of redirecting high voltage surges to the ground. The input signal from each CT and VT is connected to a transient voltage suppression (TVS) diode to clamp the over-voltage. Additionally, clamping circuits are required to restrain incoming signals within safe levels, preventing them from surpassing the input range of the processor's ADC. Following the TVS, each input is equipped with a balanced RC filter that serves as a low-pass filter to eliminate high-frequency noise interference and reduce aliasing. Matched source resistance in the positive and negative paths enhances common-mode noise rejection.

Instrumentation amplifiers are crucial for mitigating undesired circuit noise by exhibiting a high common-mode rejection ratio (CMRR) to eliminate common signals across all IC pins. The instrumentation amplifier used in this design is Texas Instruments' INA828 [36] which offers a very high input impedance. The gain for INA828 can be set from 1 to 1000 by varying the value of a single external resistor. The typical secondary current ratings employed in medium voltage current transformers are 1 A or 5 A. The growing popularity of CTs featuring 1 A secondary windings can be attributed to their capacity to reduce the sizes of transformers and secondary cables for longer cable distances. The gain control unit provides a means to select the current ratings (1 A/5 A). This selection is accomplished via a software program deployed on the main processor that controls the utilized DG467 [37] analog switch.

A low-pass filter is employed on every analog input channel to remove high-frequency noise interference and reduce aliasing. A 3rd order low pass Butterworth filter is used as an analog anti-aliasing filter. A cut-off frequency set relatively high compared to the nominal frequency yields a maximally flat magnitude response and a phase shift very linear around the fundamental frequency. Fig. 9 shows the magnitude and phase response of the implemented 3rd order low pass Butterworth filter. As illustrated, for frequencies below 1 kHz, the design generates a unit gain flat response. In this work, 32 data samples are captured during each cycle. 15 harmonics are extracted for the incoming analog signal. By changing a few circuit parameters, the filter can also be made to encompass a larger harmonics set.

A resistor divider network is used to shift the level of the incoming signal to appropriate values. Fig. 10 shows an incoming signal being shifted with a DC offset of 1.5 V. OPA196 [38] operational amplifier is utilized as a high-resolution ADC driver.

2.6. Processor module

The processor module is the core of the protection relay, where all the protection and communication codes are programmed into the STM32MP157 microprocessor. The STM32MPU kit used as a reference only supports a single ethernet interface. Hence, the reference processor design for this kit has been modified to incorporate two additional ethernet interfaces. The overall functional block diagram for the developed processor module is provided in Fig. 11.

The main processor circuitry in the developed adaptive protection relay includes the following primary components:

- *Microprocessor*: It executes tasks such as analog to digital signal conversion from the analog input module, compares current and voltage values to set thresholds and takes tripping actions, and manages communication and HMI. It is also responsible for handling the implemented multi-agent system-based adaptive protection schemes.
- *Data Storage*: The relay is equipped with various forms of memory, such as RAM and flash memory, to store instructions and data. These storage units aid the CPU in quickly accessing data and instructions, thereby improving the performance of the relay.
- *Clock*: It produces a consistent pulse to synchronize the CPU and other components' operations.
- *Interfaces*: The processor module has interfaces to the digital input and output modules, power supply, analog input, and HMI modules. It also incorporates ethernet interfaces to communicate with other relays and SCADA systems. This enables the relay to exchange information with other devices and coordinate protection and control actions. The developed processor module in this work supports three ethernet interfaces for various communication protocols, such as IEC 61850 MMS, GOOSE, SV, Modbus TCP, and IEC 60870-5-104.

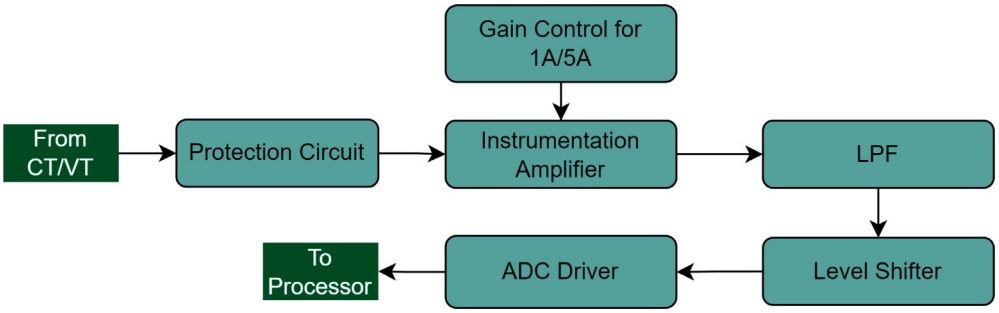

Fig. 8. Functional blocks for the analog input module.

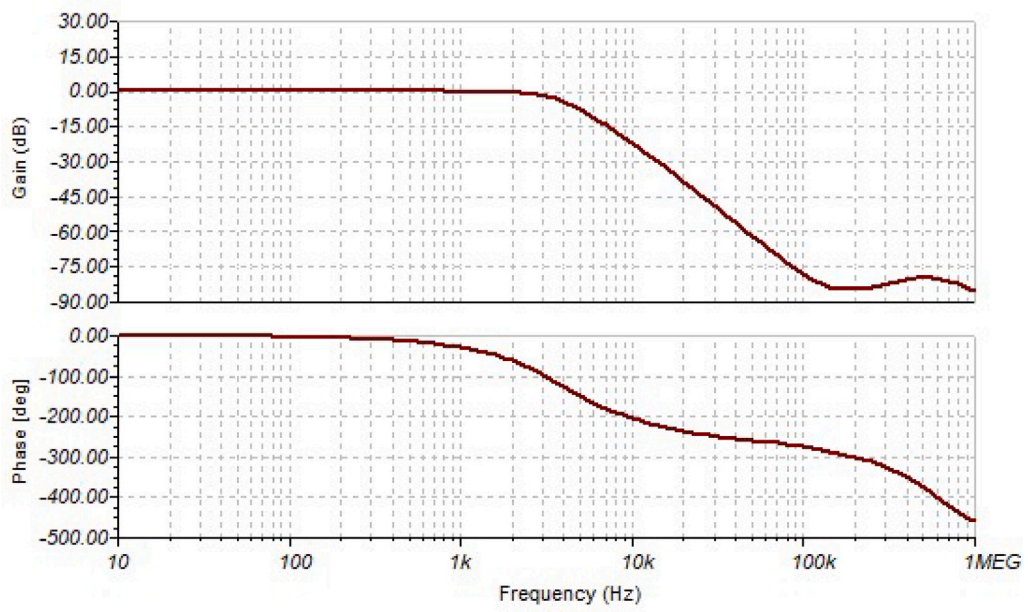

Fig. 9. Bode plot for 3rd order low pass Butterworth filter.

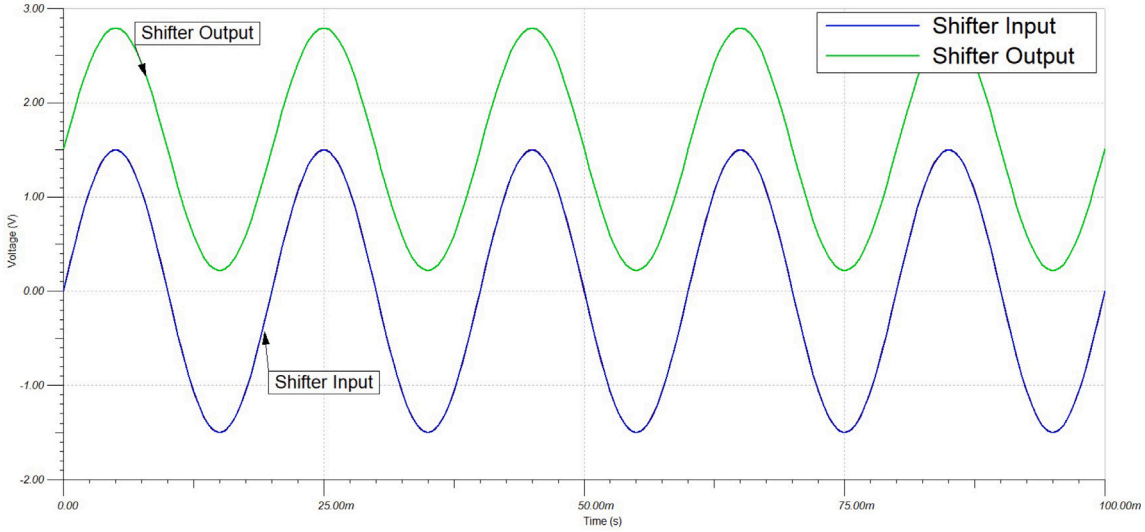

Fig. 10. Level shifter with 1.5 V DC offset.

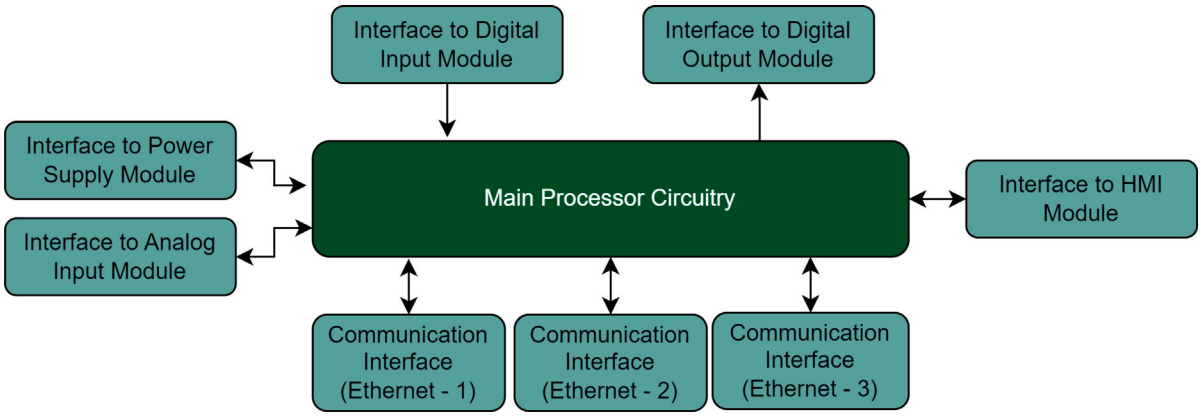

Fig. 11. Functional blocks for the processor module.

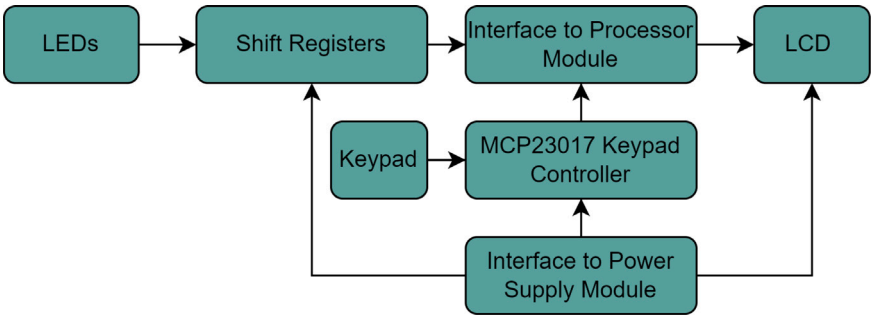

Fig. 12. Functional blocks for the HMI module.

2.7. Human–Machine Interface (HMI) module

The HMI module handles user interface features for viewing and configuring the protection relay. It typically includes a keypad, an LCD, and LEDs. The overall functional block diagram for the developed HMI module is provided in Fig. 12. Keypads are used to enter commands and navigate through the relay's menus. The LCD shows the status information and measurement values, and the LEDs indicate the relay's various statuses, including readiness, trip execution, and more.

This module is an essential component of the protection relay that allows users to interact with the relay's internal parameters. Users can get real-time data as well as past event logs. The user can also configure parameters such as protection settings, IP addresses, rated current selection (1 A/5 A), and more via HMI. In this work, an I2C communication protocol functionality via MCP23017 IC [39] to monitor keypad status has been successfully implemented. The utilized 128 × 64 LCD is programmed to show the relay's parameters, like protection settings and acquired measurements. Utilizing shift registers is a common approach to expanding the number of I/O pins on a microcontroller. Hence, SN74HC595 [31] 8-Bit shift registers have been utilized to control the LEDs.

3. Design and testing of the adaptive protection relay

As outlined in Section 2, the developed adaptive protection relay consists of multiple modules, each with designated functions. Thorough testing has led to the final refinement of every module. Preliminary design simulations have been performed using software tools such as Tina-TI, Proteus, Multisim, and PSpice. Subsequently, practical implementations and tests have been carried out on the preliminary PCB designs. The final versions of each module's PCB have been designed upon achieving the desired outcomes. The overall schematic design for all the modules is provided in Fig. 13. The PCB designs for all the modules are also illustrated in Fig. 14. Altium designer software is utilized to design the schematics and PCBs of each module.

The analog input module amplifies and filters the incoming signal from the current and voltage transformer and then shifts it to a range acceptable by the microprocessor. The developed adaptive protection algorithm analyzes the captured signal and takes action accordingly. Various tests have been conducted, including adaptive protection coordination among relays via the IEC 61850 GOOSE communication protocol, evaluating the inverse time characteristics, and more. Inverse Definite Minimum Time (IDMT) relay operation signifies that the time it takes for the protection relay to trip is inversely correlated with the magnitude of the fault current applied.

In an adaptive protection case, relays coordinate their actions by sharing status and setting values in cases of network configuration changes and fault occurrences. The developed adaptive protection relay is programmed as the primary relay for demonstration.

3.1. Network configuration change

The digital input pins on the developed adaptive protection relay are configured to get the status of circuit breakers (CBs) or switches corresponding to network configuration changes, such as the addition or removal of sources or loads in the substation. To detect changes in operating conditions, the implemented multi-agent system-based adaptive protection approach continuously monitors the statuses of the corresponding digital input pins while keeping track of notifications regarding network configuration changes from other relays via GOOSE messaging. Existing protection relays offer support for only a limited number of setting groups. In contrast, the implemented multi-agent system-based adaptive protection scheme overcomes this limitation by achieving adaptive setting groups based on changes in the integrated loads and sources. Hence, the utilization of multi-agent systems enhances relay adaptability by enabling the incorporation of multiple

Fig. 13. Schematic designs of the hardware modules.

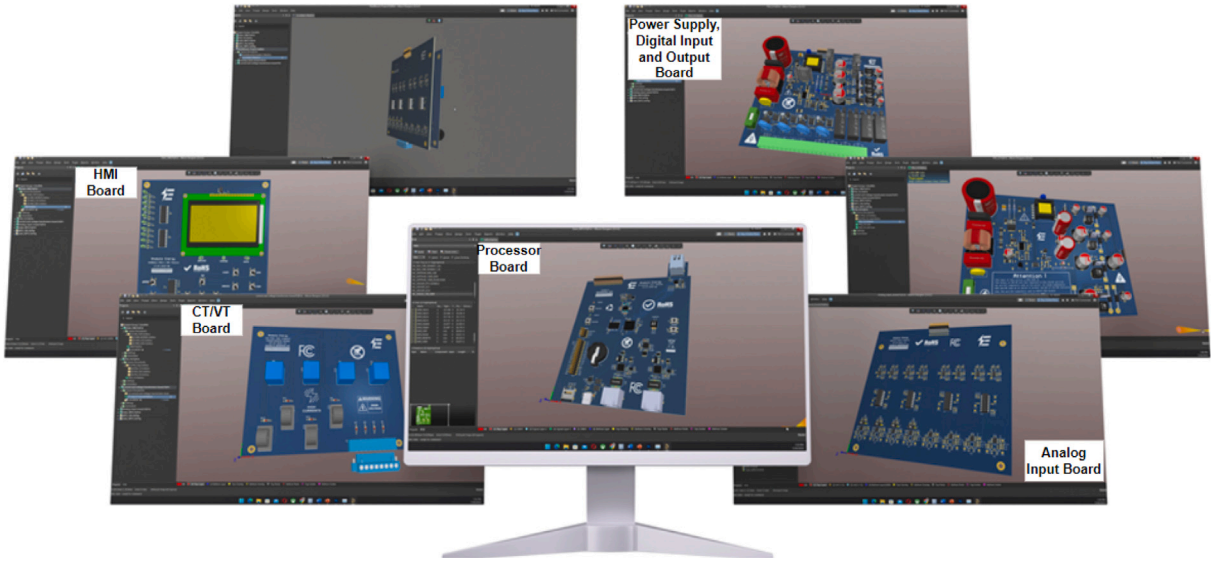

Fig. 14. PCB designs of the hardware modules.

setting groups, thereby automating adjustments for various network conditions.

Various ANSI and IEC operating curve types have been implemented, allowing the user to select the desired operating curve type. Using the IEC normal inverse curve formula shown in Eq. (3), the primary relay calculates its operating time that will be used for coordination by the upstream relays to determine their respective time multiplier setting (TMS) values.

$$t_{prim} = \frac{TMS * 0.14}{(\frac{I_{primf}}{I_{ppick}})^{0.02} - 1} \tag{3}$$

Where:

TMS = Time Multiplier Setting

t_{prim} = Operating time for primary relay

I_{primf} = Initial coordination fault current value

I_{ppick} = Primary pickup current value

The TMS, initial coordination fault current, and pickup current assumed in this demonstration are 0.1, 5 A, and 1.2 A, respectively (considering a 1 A CT). It should be noted that the current values are from the secondary side of medium voltage current transformers. The calculated operating time using Eq. (3) is 0.484 s. The primary relay transmits this value to the upstream relays using the IEC 61850 GOOSE communication protocol, as depicted in Fig. 15. The NetConfig value indicates the network configuration status. Upstream relays check this value whenever a new GOOSE message arrives and update their settings if there is a change from the previous NetConfig value. Updating the settings is not required if it is the same as the previous value. The Blocking value indicates the occurrence of a fault. Upstream relays check this value whenever a new GOOSE message arrives and be on standby if this value is TRUE. Coordination Time Interval (CTI) denotes the minimum duration between a primary device and its upstream backup's operating time [24]. The CTI value assumed for demonstration is 0.14 s.

Based on this GOOSE message, the upstream relay utilizes Eq. (4) to determine its time multiplier setting (TMS_{ups}) and uses the obtained

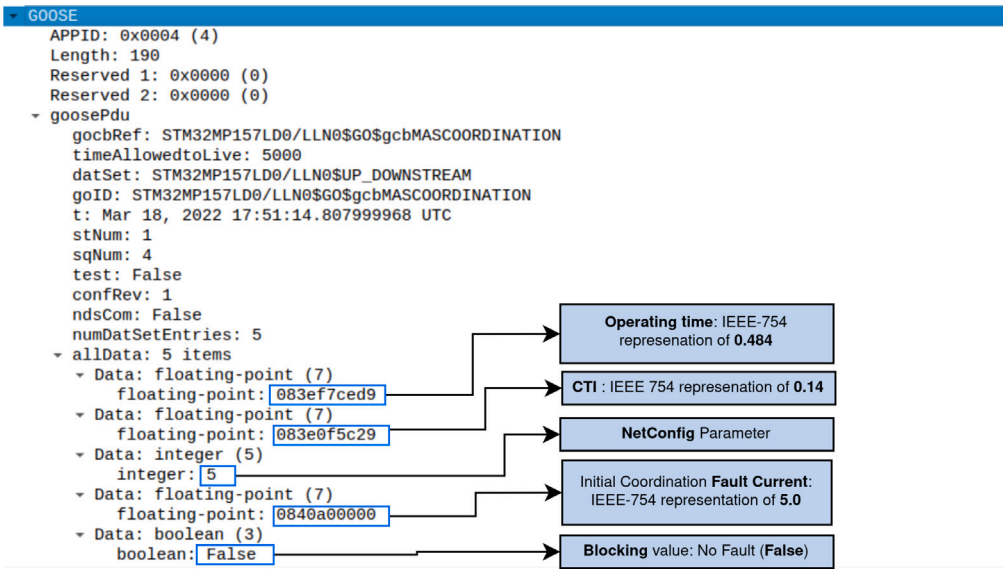

Fig. 15. GOOSE message sent by primary relay.

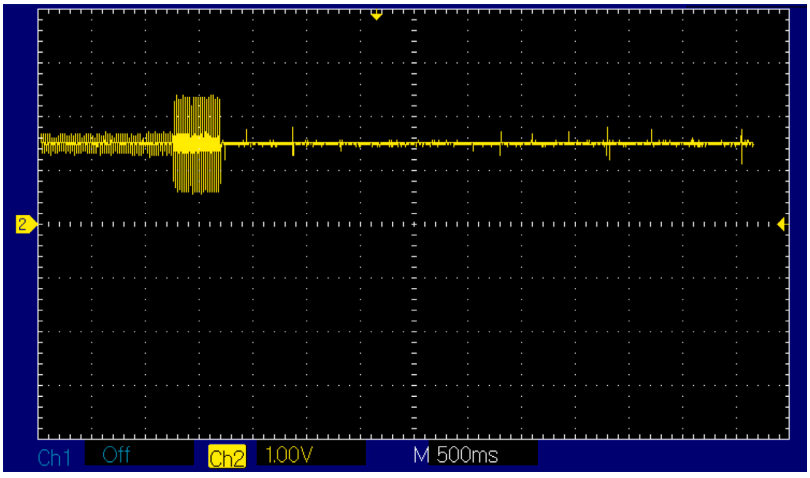

Fig. 16. Tripping for a 6.5 A fault current.

value to calculate its operating time. It also sends a GOOSE message comprising its new settings to its upstream (backup) relay with a structure similar to the primary's GOOSE message in Fig. 15. Consequently, the manual reconfiguration of each relay required in existing numerical relays for such changes is avoided by adopting the developed adaptive protection scheme [23].

$$TMS_{ups} = \frac{t_{prim} + CTI}{\frac{0.14}{\left(\frac{I_{primf}}{I_{upick}}\right)^{0.02} - 1}} \tag{4}$$

Where I_{upick} : Pickup current for the upstream relay

3.2. Fault occurrence

Several fault currents have been applied to evaluate the implemented adaptive protection schemes and inverse time characteristic features. Among the various faults applied, a few are listed as follows:

- ***6.5 A fault current***: When a fault of 6.5 A is applied in the primary protection region, the main tasks done by the primary relay are determining the operating time and notifying the upstream relays of the situation. As a notification, the primary relay sends an IEC 61850 GOOSE message similar to Fig. 15 by changing the blocking status to TRUE. This action ensures that the upstream (backup) relay does not trip and stays on standby mode while the primary relay handles the fault. As illustrated in Fig. 16, a DC offset of 1.5 V is introduced onto the incoming 50 Hz signal acquired via the current transformer to keep it in the acceptable input signal range. Eq. (5) yields the operating time, which is approximately 0.41 s for a 6.5 A fault current. As mentioned above, the TMS and pickup current used for this demonstration are 0.1 and 1.2 A.

$$t_{oper} = \frac{0.1 * 0.14}{\left(\frac{I_{meas}}{1.2}\right)^{0.02} - 1} \tag{5}$$

Where: t_{oper} = Operating time
I_{meas} = Measured fault current value
Hence, the tripping procedure is initiated to isolate the faulty section upon detecting the fault. The processor will start the delay timer based on the operating time while continuously monitoring the faulty condition. If the fault persists beyond the set delay duration, the processor will transmit a trip signal through the digital output module. As observed in Fig. 16, when the tripping action is executed, the output will be a flat 1.5 V DC, which is the offset value indicating the successful isolation of the faulty section.

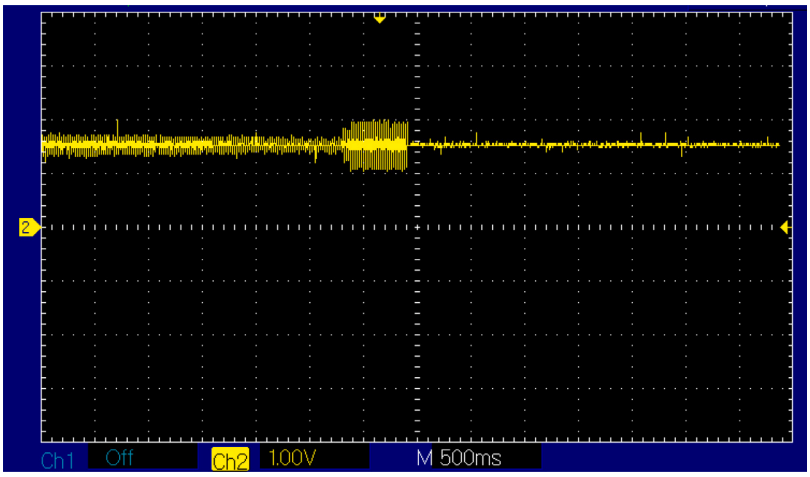

Fig. 17. Tripping for a 4 A fault current.

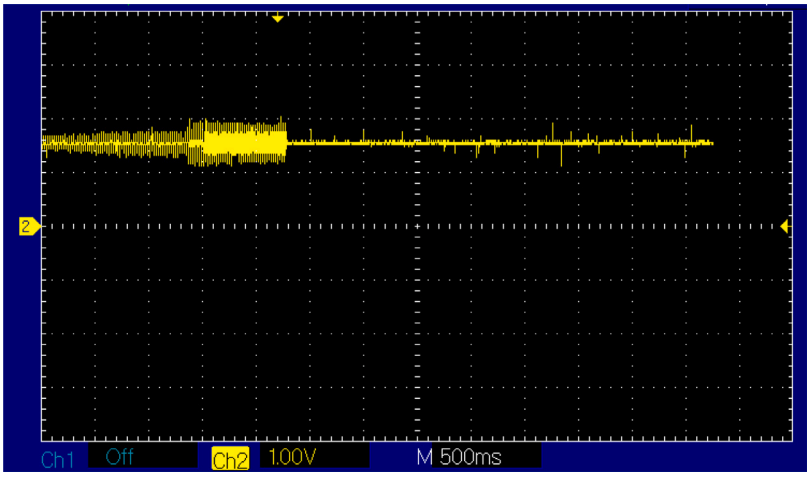

Fig. 18. Tripping for a 2.5 A fault current.

- ***4 A fault current***: Similar to the case of 6.5 A, the primary relay sends a GOOSE message to the upstream relay, besides determining the operating time, which is around 0.57 s for an applied 4 A fault current. This value exceeds the operating time calculated for the 6.5 A fault current, complying with the inverse time characteristics. Similarly, the tripping procedure is initiated to isolate the faulty section upon detecting the fault. The processor will commence the delay timer while continually observing the fault's status. The processor will send a trip signal via the digital output module if the fault sustains when the allotted delay time expires. The tripping action after approximately 0.57 s can be observed in Fig. 17.
- ***2.5 A fault current***: The calculated operating time for a 2.5 A fault current is approximately 0.94 s. The primary relay also sends a GOOSE message that helps set the upstream (backup) relay on standby. As expected, the calculated operating time exceeds those calculated for the 4 A and 6.5 A fault currents. Detection of a fault causes the initiation of the tripping procedure. If the fault persists beyond the calculated delay duration, the processor will issue a trip signal using the digital output module, as shown in Fig. 18.

In the same manner, several tests have been conducted for various fault current values, and the resulting values are shown in Fig. 19. As can be noticed, these results agree with the standard inverse time characteristics, indicating that higher fault currents require a shorter trip time delay.

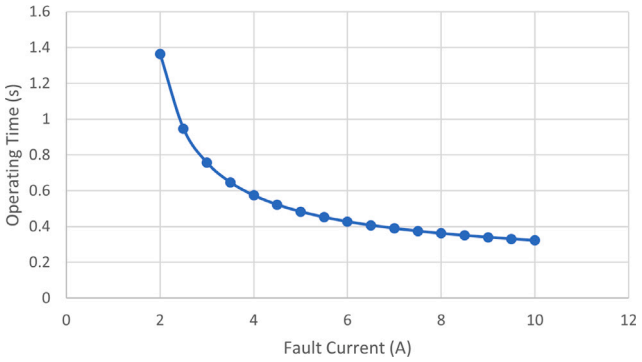

Fig. 19. Inverse time characteristics.

On the other hand, relays in the opposite direction of energy flow use GOOSE messaging to send follow-me signals to notify each other of fault occurrence [24]. The basic coordination steps can be summarized in Fig. 20.

CASE - I Initial Coordination (Primary) Relay

if *NetConfig* has changed **then**
  Calculate *Operating_time*
  Send GOOSE Message to backup ▹ Blocking set to FALSE
end if
if *Fault* occurs **then**
  Send GOOSE Message to backup ▹ Blocking set to TRUE
  Calculate Operating (delay) time
  Initiate trip sequence
end if

CASE - II Upstream (Backup) Relay

if $NetConfig\_previous \neq NetConfig\_current$ **then**
  Update protection settings
  Send GOOSE Message to upstream ▹ Blocking set to FALSE
end if
if *Blocking* is TRUE **then**
  Calculate *Operating_time*
  Wait for downstream relay to clear fault
  if *Fault* is not cleared **then**
    Initiate trip sequence
  end if
end if

CASE - III Opposite Relay

if *Fault* occurs **then**
  Calculate *Operating_time*
  if *Follow_me* is TRUE **then**
    Wait for opposite relay to clear fault
    if *Fault* is not cleared **then**
      Initiate trip sequence
    end if
  else
    Send GOOSE Message to opposite relay ▹ Follow-me set to TRUE
    Initiate trip sequence
  end if
end if

Fig. 20. Basic coordination among MAS-based adaptive protection relays.

Fig. 21 depicts the input and output signals of the digital input module captured via an oscilloscope. Digital inputs can be used as status indicators for switches, circuit breakers, or signals from other relays. A 24 V DC voltage input applied is optimized to 3.3 V DC voltage acceptable by the digital input pin of the microprocessor. As illustrated in Fig. 21, for the absence of a digital input signal, the comparator outputs 0 V, while it yields 3.3 V, indicating the high status of the input signal.

The complementary part I- firmware article has thoroughly examined the adaptive protection scheme utilizing a multi-agent system. It offers an elaborate analysis of the testing process and delves into the coordination among relays during network configuration changes and fault occurrences. It also discusses the IEC 61850 GOOSE communication protocol-based coordination among relays utilizing the MAS approach. Moreover, it elaborates on the key algorithms involved in the developed MAS-based adaptive protection.

4. Conclusion

Numerical relays play an integral role in the efficient operation of electrical grids. With the insertion of multiple feeders and sources, existing numerical relays require an effective way of managing the bidirectional flow of energy. The changes in network configurations due to the addition and removal of sources and loads can be handled seamlessly by integrating an adaptive protection scheme. This article has explored the hardware structure employed in designing an adaptive numerical relay. It comprises hardware modules such as the power supply, processor, digital input and output, analog input, and Human–Machine Interface (HMI). The STM32MP157 microprocessor has been utilized as the main CPU for handling the relay's firmware with precision and reliability. The incorporation of explanatory flowcharts for each hardware module's functionality provides a comprehensive understanding of their interconnected operations. Furthermore, the provided

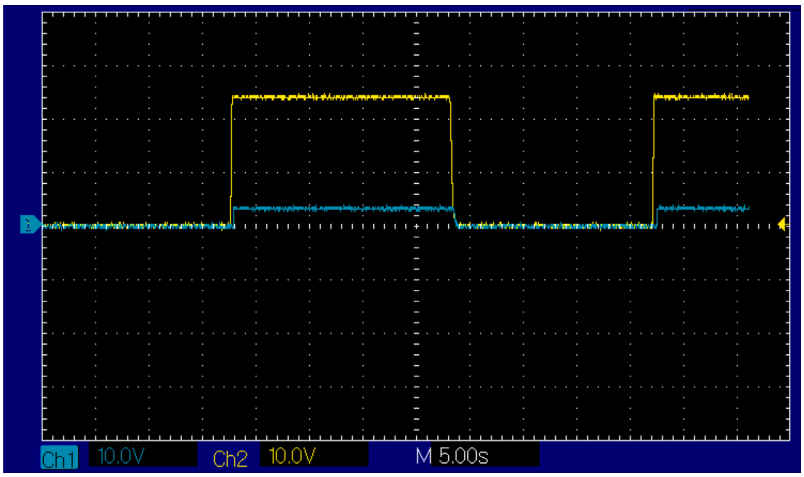

Fig. 21. Input and output signals of the digital input module.

schematics and PCB layouts indicate the feasibility of deploying these modules in real-world scenarios. This article provides several tests comprising adaptive protection coordination and conditioning of digital input signals. The achievements of this work can significantly contribute to the advancement of numerical relay technology and underscore the importance of an adaptive approach in addressing the challenges of modern electrical grid management.

CRediT authorship contribution statement

Abdulfetah Abdela Shobole: Conceptualization, Methodology, Software, Investigation, Writing – original draft, Writing – review & editing. **Motuma Abafogi:** Conceptualization, Methodology, Software, Investigation, Writing – original draft, Writing – review & editing. **Abdurrahman Zaim:** Conceptualization, Methodology, Software, Investigation. **Yahia Amireh:** Conceptualization, Methodology, Software, Investigation.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Abdulfetah Abdela Shobole reports financial support was provided by Scientific and Technological Research Council of Turkey.

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Data availability

Data will be made available on request.

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