Design and Test of a High-speed Flash ADC Mezzanine Card for High-resolution and Timing Performance in Nuclear Structure Experiments

X. Egea, E. Sanchis, *Member, IEEE,* V. González, *Member, IEEE*, A. Gadea, J.M. Blasco, D. Barrientos, J.J. Valiente Dobón, M. Tripon, A. Boujrad, C. Houarner, M. Jastrząb, M. Blaizot, P. Bourgault , G.de Angelis, M.N. Erduran, S. Ertürk, G.de France, T. Hüyük, G. Jaworski, A. di Nitto, J. Nyberg, M. Palacz, A. Pipidis, R. Tarnowski, A. Triossi, R. Wadsworth

***Abstract* – This board will be part of the upgrade for the new electronics for the EXOGAM2 (HP-Ge detector array) and NEDA (BC501A-based neutron detector array), therefore it was necessary to deal with the problem of providing a sampling card with high resolution for new gamma spectroscopy experiments while sampling at very high rates, with a broad bandwidth in order to preserve the shape for further analysis. Pulse shape analysis is of paramount importance in neutron detectors, such as NEDA, based on scintillators that are sensitive to γ-rays as well. High resolution and high speed are often two parameters which conform a trade-off and it is hard to achieve both simultaneously. The aforementioned constraints and the urge of building new sampling electronics to improve the signal analysis in nuclear physics experiments, led to the development of this FADC mezzanine This involves sampling rates up to 250 Msps preserving a high resolution of 11.3 effective bits in order to satisfy the experiment demands. In this work is described the design and the test bench proposed for a proper high speed ADC characterization system and the results obtained up to now.**

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F.J. Egea, A. Gadea, D. Barrientos and T. Hüyük are with Instituto de Física Corpuscular (CSIC-UV), Valencia, Spain. Corresponding author: Francisco Javier Egea Canet; e-mail: jaegea@ific.uv.es

V .González, J.M. Blasco and E. Sanchis are with Departament d'Enginyeria Electrònica (Universitat de València), Escola Tècnica Superior d'Enginyeria, Burjassot (Valencia, Spain).

M. Tripon, A. Boujrad, C .Houarner, G. de France, P. Bourgault and M. Blaizot are with Grand Accélérateur National d'Ions Lourds (GANIL), 14706, Caen, France.

M. Jastrząb is with the Niewodniczański Institute of Nuclear Physics, Polish Academy of Sciences, Kraków, Poland.

J.J. Valiente Dobón, G.De Angelis, A.Triossi and A.Pipidis, are with *INFN*, Laboratori Nazionali di Legnaro, Padova IT-35020, Italy.

G. Jaworski is with Faculty of Physics, Warsaw University of Technology, Warszawa, Poland.

R. Tarńowski is with the Heavy Ion Laboratory, University of Warsaw, Warszawa, Poland.

J. Nyberg is with Department of Physics and Astronomy, Uppsala University, Uppsala, Sweden.

A. di Nitto is with INFN, Sezione di Napoli, Napoli, Italy.

M.N. Enduran is with Faculty of Engineering and Natural Sciences, Istanbul Sabahattin Zaim University Istanbul, Turkey.

S. Ertürk is with Nigde Universitesi, Fen-Edebiyat Falkultesi, Fizik Bölümü, Nigde, Turkey.

R. Wadsworth is with Department of Physics, University of York, York, United Kingdom.

I. Introduction And Specifications

When designing high speed acquisition systems is extremely important to deal with phenomena like noise and jitter, which can degrade significantly the signal to noise performance. Normally, these undesirable effects, which might be already problematic at frequencies below the MHz, makes a major challenge to deal with them at frequencies over of hundreds of MHz [1].

As this board will be used for the EXOGAM2 and NEDA, specifications from both detectors must be satisfied. In terms of resolution, taking a look onto the specifications from the EXOGAM2 detector, since it is a gamma spectrometer built with HPGe detectors, electronics must not add extra noise which degrade the energy resolution from the HPGe detectors, therefore, energy resolution parameters are fixed from this side. For the new generation experiments, a 2.3 keV energy resolution in a 1.3 MeV range must be at least accomplished [2]. In terms of electronics, the Effective Number Of Bits (ENOB) gives the resolution parameter in terms of electronics. For the EXOGAM2 case a 11.3 ENOB resolution is demanded. By contrast, NEDA is used for gamma-neutron discrimination, a common procedure used in nuclear experimental physics, based on pulse shape discrimination. However, EXOGAM2 resolution demand is more restrictive, then NEDA works well with a 11.3 ENOB. On the other hand, the signal rise-time gives the fastest component, and for NEDA now it is much more restrictive. EXOGAM2 pulses come from the charge pre-amplifiers, where pulses with an average rise-time of 100 ns, with a 50 μs come to the FADC Mezzanine [3]. However, organic scintillators from NEDA, involve much faster rise-times, on the order of 10ns. Based on this restriction, the minimum sample rate should not be lower than 200-250 MHz for a proper acquisition. Summarizing up, it is mandatory from one side to keep intact the amplitude from the HPGe pulses, with the minimal noise addition, while dealing at the same time with the very fast pulses from the organic scintillators. Hence, it is a challenging design which combines both high-resolution with high-speed.

The way this design was approached, has been based on a choice of a commercial ADC, followed by a clock cleaner, which allows the generation of proper low-jitter sampling

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clocks and finally, the design of a full-differential analog stage, which adapts the input range to the FADC range, and compensates the effect of the baseline level by adding certain offset voltages. Besides the main parameters described above, issues like the control protocol, interface with other systems, power consumption and signal integrity have been carefully studied in order to provide an optimal performance with the most simplicity [3].

Among other specifications, 4 FADC mezzanines will be mounted onto a motherboard, the NIM-crate-based NUMEXO2 digitizer, therefore so does the FADC Mezzanine in proportion. Each digitizer is capable to process information from 16 channels and can plug up to 4 Mezzanines. Therefore, each FADC Mezzanine has to contain 4 channels [3].

II. FADC MEZZANINE DESIGN

A. Main Devices Choice (FADC, PLL, DACs, OPAmps)

Once the specifications in terms of resolution, sampling rate and channels area known, the first task is to choose the main devices. For our case, the sampling rate, resolution, and number of channels finally led to the choice of the FADC from Texas Instruments *ADS62P49,* a 14-bit dual-FADC, capable to sample up to 250 MHz. For this FADC mezzanine board, 2 devices are used for 4-channel acquisition [6].

Assuming the input signal bandwidth and resolution , the clock jitter must be less than 1ps [1]. *LMK03001C* PLL (Phase-locked-loop) from National Semiconductors combines a jitter performance of 400 fs with a partially integrated filter and integrated VCO. Unlike the FADC *ADS62P49*, which uses SPI, *LMK03001C* uses the µWire protocol, but very similar [7].

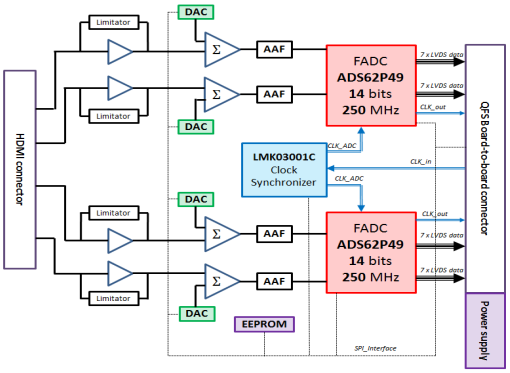

Fig. 1. FADC Mezzanine block diagram, including the most important blocks, such as the FADC device, PLL, DACs, operational amplifiers and connectors.

When the FADC and PLL are chosen, it rest to choose the DACs, and the analog stage topology mainly. According to the specifications, dynamic offset signal must be added for two different proposals: the usage of the full-scale differential FADC range and the baseline restoration. This has been implemented by adding a dual-16-bit DAC, concretely the *DAC8532* from Texas Instruments. A higher number of bits has been chosen for the DAC in order not to add extra noise, besides, its low-power and SPI protocol, makes it compliant with the FADC and PLL control [8].

The FADC range needs to be properly mapped with the input range for different energy ranges (5 MeV and 20 MeV), and at different bandwidths (EXOGAM and NEDA bandwidths are different too), with a minimal noise addition. Hence, an analog stage has to be added taking into account parameters such as the amplifier bandwidth, noise spectral densities and the gains allowed. A topology combining *AD8002*, *AD8139* and several passive components, seems to be the optimal for this application [9-10].

Other secondary but not less important devices required are the LDO regulators, connectors, SPI current drivers used to provide current enough to all the devices and a small EEPROM used to store information concerning the Mezzanine ID. In the Fig. 1, a block diagram shows the global functionality, where all the devices mentioned above have been included.

B. Power Supply, Connectors and Control.

FADC, PLL and DAC need to be power-supplied from clean voltage regulators, like LDOs (Low Dropout Regulator). Besides, if possible, the supply voltages and must be compliant so that too many different voltage and several control protocols increase the complexity and the amount of extra devices.

On this way, based on the input voltages obtained from the connector placed on motherboard, we find: +6, -6, +4 and +3.3 V, according to the schema depicted in Fig.2, where also the devices used are shown.

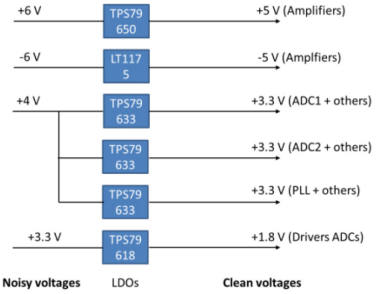

Fig. 2. Power supply distribution diagram, where it is detailed the voltages taken from the motherboard and which voltage are converted to.

Some of the power planes, even if they carry the same voltage, have been preferably isolated, for example, FADC analog and PLL power supplies. The reason is that both of them are noise-critical. On the other hand, other devices working at 3.3V do not need an extra power plane and can be connected either to the FADC or the PLL power plane. Regarding the power consumption, it has been obtained a total power consumption around 6 W for each mezzanine (assuming a sampling frequency of 250 MHz), where mostly it is consumed in the FADC device and LDO regulators.

The FADC Mezzanine communicates through connectors placed at the FADC input with the previous modules and board-to-board connectors, to be plugged onto the carrier motherboard. These connectors have been chosen based on the type and number of signals being carried, as well as the bandwidth and connector size. The input connector carries

analog high-speed signals and its choice has been based on several tests applied to different cables. These tests included crosstalk, bandwidth, electromagnetic compatibility and reflections. Hence, the *HDMI* cable, was preferred amongst other connectors such as the *HDR PoCL* camera cable or the *MDSM* coaxial cable, which were tested too. However, depending on the *HDMI* version, shielding and bandwidth are different, so that different *HDMI* versions might be used for EXOGAM2 and NEDA. The version for this mezzanine includes 4 differential pairs and 6 single-ended lines. It is expected to use different *HDMI* versions for different detectors.

The board-to-board connector has to count on pins enough to communicate the FADC Mezzanine with the motherboard. Inspecting the block diagram from Fig.1, FADC data outputs contain 4 channels with 7 differential output data, used to multiplex the odd and even bits from each differential pair. This increases the number of data lines up to 56. Adding the differential clock outputs and the clock inputs, this sums 6 signals. Likewise, SPI control lines (SCLK, MISO , MOSI + 8 CE), 2 extra single-ended (FADC_RESET and PLL_SYNC), and 4 reserved differential pairs for a possible future use. These lines sum up to 56 + 6 + 11 + 2 + 8 = 83 signals, and are all detailed in the Fig.3. The connector chosen is the *QFS-26-04.25-L-D-PC4*. The PC4 ending makes reference to the addition of special pins for power supply board-to-board transmission, used to drive all the voltages and a ground path for each power supply. 2 connectors are required to transmit all the set of signals to the motherboard.

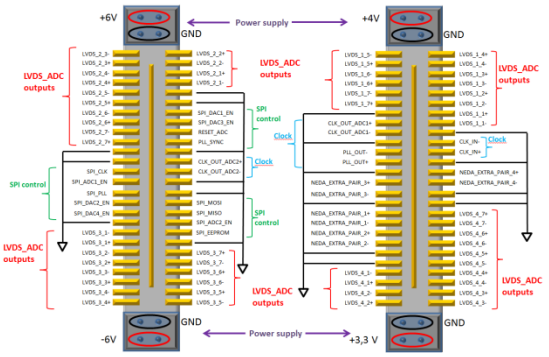

Fig. 3. Board-to-board connection from the FADC Mezzanine to the test board and motherboard, based on the connectors QFS-026-L-D-PC4.

Some of the devices require a set of commands which need to be properly setup before starting up the FADC mezzanine. Devices such as the PLL, FADC or DACs include an SPI receiver which allows this setup task. 8 lines command the election of the device under control, while the data and clock lines are shared. The mezzanine is provided with current buffers *74LVC2G126* to drive current enough through the clock and input data lines. As well, for the data readout, these drivers can keep at high-impedance the unused outputs, allowing the direct connection of the outputs from both FADCs and the EEPROM.

C. *Analog Stages Topology*

The most critical stage in terms of resolution and noise is the analog stage preceding the FADC input. This stage, based on the full-differential amplifier AD8139 and the current-feedback amplifier AD8002, must achieve the input-to-FADC voltage mapping for different energy channels, at 5 MeV and 20 MeV. The extra noise for these stages should not overcome 1 LSB. The FADC range is ±1V differential, plus a 1.5V common mode. For EXOGAM2, the previous stage establishes the energy-to-voltage mapping with a sensitivity of 200mV/MeV. Hence, the input ranges are from ±1 V for 5 MeV and ±4 V for 20 MeV.

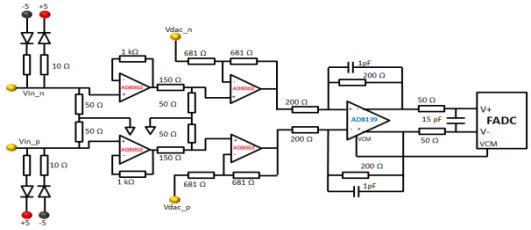

Fig. 4. Analog stage detailed topology. The signal path from the HDMI connector to the FADC mezzanine is sketched.

According to the Fig.4 shown above, the analog stage is divided in three sub-stages, to mention, a voltage follower, a gain plus offset part, and the full-differential amplifier. The first stage includes the *AD8002* used as a follower, the terminators, and protection diodes to avoid overvoltage peaks higher than ±5V avoiding damage on the analog amplifiers. The follower is used to isolate the 50Ω terminators to the next stages, providing a very high-impedance to the next stage.

The second part is made up by a second *AD8002* amplifier, a voltage divider connected to the non-inverting input, and a DAC input connected to the inverting input. The energy range can be changed at the voltage divider, where for 20 MeV it divides the gain by 4, and left to 1 (voltage divider disassembled) when the energy range is 5 MeV. At the FADC input, the -1V level must be map to the baseline level, and +1V is mapped to the highest peak. Taking a look on the Fig.4, the second AD8002-based stage contains a gain G=2 for the non-inverting input and a G=-1 for the inverting input. In order to get this range, offset values adjusted to -0.5 V offset for the non-inverting input and +0.5 V at the inverting input, getting this way the desired differential range.

The last stage is used with a full-differential amplifier *AD8139*, in order balance the differential stage, while adding as well a common-mode voltage, mapping it directly into the FADC range. An additional fourth stage, maps the DAC 0-3.3V values to the voltages added at the offset stage, which are mapped between ±1V, using the AD8662 [11].

D. *Layout Tips and Prototype Production*

In this section it is going to be described briefly the layout issues which have been followed for this design.

All the points mentioned on the previous section make reference to the design of one FADC mezzanine, but, the carrier motherboard will be fixed into a NIM crate containing each 4 Mezzanines. The size of the NIM crate is 183 mm wide

x 255 mm long. Therefore, the NIM crate imposes a size restriction in terms of width, where 4 boards must fit leaving a millimetric gap in between, leading to a width 42 mm. The length, even if it has a bigger degree of freedom, is still restricted as the devices on the motherboard make an obstacle, where the maximum length holds restricted too. The choice finally has been set to a 100mm length. Furthermore, a couple of slots have been left at the mezzanine front-panel sides, in order to place LEMO connectors on the front panel.

The layer structure uses 10 layers, where 4 are used as signal layers, 3 ground layers and 3 power planes, where most of the traces on TOP and BOT form differential microstrips and require a GND plane adjacently. Considerations about differential routing are used, with strong-coupled traces at 100Ω differential impedance. In addition, the FADC differential data outputs must be length-matched with a 1mm to avoid phase shift on any differential pair [12].

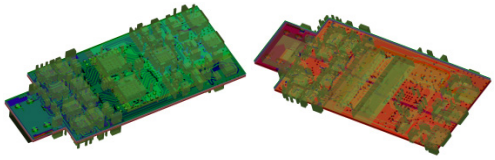

Fig. 5. Left. FADC Mezzanine finished layout TOP 3-dimensional view. Right. FADC Mezzanine finished layout BOTTOM 3-dimensional view.

Further techniques such as thermal vias connected to thermal pads, used to improve the heat dissipation, are used in some devices (FADC and PLL), as well as low-impedance traces for the analog amplifier inputs, reducing this way the stray capacitance. A layout schema can be seen on the Fig.5, where the 3-D model has been extracted using the PCB Editor, version 16.3 from Cadence.

III. FADC MEZZANINE TESTBENCH

This section discusses the elements regarding the FADC Mezzanine test bench, including the materials, as well as the firmware and data analysis algorithms which have been used.

A. Test Bench Hardware and Tools.

The FADC Mezzanine Testbench requires a device capable both to read and monitor the digitized data from the FADC Mezzanine. To achieve this goal, a ML605, containing a Virtex6 FPGA [5] has been used. This device provides resources enough to acquire data at high-speed sampling rates as well as the inclusion of a Chip Scope Pro block for analysis and monitoring proposals.

Additionally, an intermediate board called FADC test-board links the data from the FADC Mezzanine to the ML605. Besides, it provides power supply by adding DC / DC converters to generate the extra voltages, taking ±6V from the power supply. The power supply used for this Testbench is the FAC-662B from Promax. In addition, the FADC Mezzanine is able to be controlled either from the current ML605 or from an alternative board using a Virtex5, the ML507. This selection can be done by a jumper selection.

An additional small board links the SMA / BNC connectors which usually generators are provided with, making it compliant with the HDMI connector. On the Fig.6, it is shown the full test bench with the respective blocks already mentioned.

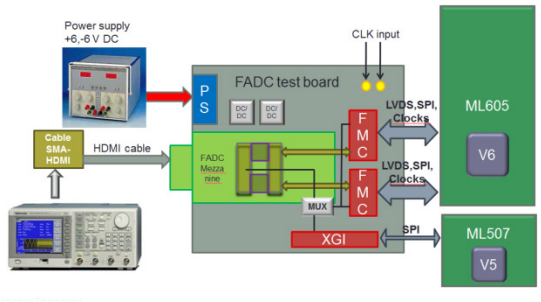

Fig. 6. Test bench block diagram.

The function generators which have been used for this set up are the Tektronix AFG3252, and the Agilent 33522A. However, for the energy histogram, the BNC PB-4 pulse generator was preferred since the pulse signals are generated more cleanly.

Among the software tools which have been used can be listed as follows:

- Xilinx Platform Studio (XPS) / ISE Xilinx tools, have been used to describe the embedded µBlaze processor inside the Virtex6 device as well as the additional cores accompanied with it, like the ISERDES or the energy calculus blocks.
- Chip Scope Pro. The virtual scope core is inserted as well inside the V6 using either XPS or ISE, where the signals can be monitored. Another interesting operation is the possibility to export files which can be read by another software, such as Matlab.
- Matlab. By exporting the data from Chip Scope Pro to Matlab, the FADC Mezzanine performance can be tested by implementing histograms, FFTs, algorithms for INL / DNL analysis, etc.

B. Firmware

Basically the firmware can be divided in two big parts. On one hand, the cores which are used to acquire and monitor data, and, on the other hand, the control and setup parts which are embedded in a µBlaze processor.

To understand the data collection and its deserialization, we must understand how the FADC delivers the digitized samples to the FPGA. Each FADC Mezzanine output is distributed in 7 differential pairs, in which each line contains multiplexed data from two consecutive bits, f.e. the line 0 carries the bit 0 and 1, line 1 carries the bit 2 and 3, etc. where the even bits are digitized during the rising-edge, and the odds on the falling-edge. At the Xilinx IP ISERDES block output, the data has been reordered in 14-bit samples. Once the data has been reordered, the samples can be monitored on Chip Scope Pro, in groups of even-odd samples. The firmware block diagram and deserialization is shown on the Fig.7.

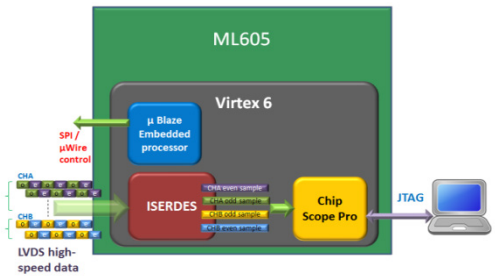

Fig. 7. Firmware block diagram used for the signal analysis. It contains the FADC setup, the data deserialization and the monitoring by using the Chip Scope Pro.

The part makes reference to the µBlaze embedded processor, used to configure the FADC Mezzanine registers based on SPI/µWire. An embedded processor was preferred due to the programming sequential process, which simplifies the design and makes it more flexible. By setting up the FADC Mezzanine, the internal registers from the FADC, PLL, DACs and EEPROM are configured properly, configuring parameters such as the sampling frequency and delay between data and clocks. Also, the LVDS / CMOS FADC output, as well as gain and offset corrections among others. The task firstly sets up the configuration of the FADC and PLL, and afterwards, updates continuously the DAC values which are summated at the analog stage.

C. Measurements

The measurements concerning the evaluation of this FADC Mezzanine are basically the standard measurements used to characterize any A/D chip. In addition, parameters used in nuclear physics such as the FWHM were measured too. Into this sub-section all the measurements which have been applied will be described as well as the procedure and algorithms used.

1) Noise Performance.

The most important parameter, concerning the resolution demands is the noise performance. To measure noise, no input is used, leaving the FADC to acquire the noise generated from the analog stages and the FADC itself. To quantify the noise, standard deviation σ and SNR are used. Taking the half-FFT from Matlab, the SNR and FFT noise floor are related by:

$$SNR = 20\log\sqrt{2}\sigma V_{lsb} \quad (1)$$

$$NF = -SNR - 10\log\frac{N}{2} \quad (2)$$

Where σ is the noise standard deviation, V_{lsb} is the LSB voltage, and N is the number of points used to perform the FFT. The $\sqrt{2}$ arises from when taking only half FFT, in order to compensate the energy term, which in terms of amplitude leads to $\sqrt{2}$.

2) Effective Number of Bits (ENOB).

ENOB, together with the noise performance, are mandatory to determine the FADC performance. The main difference is that ENOB contemplates the distortion as well, based on the SINAD (Signal to noise and distortion ratio) calculus, a more general approach from the SNR. The expressions (3),(4) and (5), define the parameters, where the E terms are referred to the signal energy,

The procedure used to calculate the ENOB consists to get different sinusoids at different input frequencies, sampled at 100 and 200 MHz, establishing the ENOB as a function of the frequency. [13]

$$SNR = 10\log\frac{E_{signal}}{E_{noise}} \quad (3)$$

$$SINAD = 10\log\frac{E_{signal}}{E_{noise}+E_{distortion}} \quad (4)$$

$$ENOB = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{Full-scale\ amplitude}{Input\ amplitude}\right)}{6.02} \quad (5)$$

SINAD is usually calculated by separating on the frequency domain the signal energy from the noise and distortion energy. To separate the signal from the rest of bins, it can be done by summating the bins around the maximum peak over the FFT.

3) Differential and Integral Nonlinearities.

DNL (differential nonlinearity) evaluates the width of the LSB steps comparing them to the nominal LSB width. On the other hand, INL (integral nonlinearity) measures how the measured transfer function fluctuates, comparing it to an ideal linear transfer function [13]. The common procedure to evaluate these parameters is by performing a code density test with a large number of samples, using a triangular or saw-tooth waveform across all the possible codes [13]. However, when the number of bits is larger than 12, it is preferred to use the sinusoidal waveforms since they can be generated with less distortion. The algorithm used for INL and DNL measurements is based on a code density test as well, with certain modifications consisting on the transformation of the sine PDF (Probability density function) in order to get what it would be a normal density test.

When using the sinusoidal histogram method, three issues must be watched out: number of samples taken, input frequency and amplitude. A comprehensive nonlinearity test can be covered only if all the codes are present, therefore the input signal must cover the full-scale range. On the other hand, the input frequency needs to be accurately chosen in order to randomize the histogram, avoiding repetitive sampling at the same point in each period. From the time-domain point, this fact establishes to sample uniformly from 0 to 2π, hence, collecting samples at all the phases. When choosing an input frequency, the expression (6) must be used, where f_{in} is the input frequency, f_s the sampling frequency, M the number of samples in a record and D the number of cycles per record.

$$\frac{f_{in}}{f_s} = \frac{D}{M} \quad (6)$$

The point is to establish a ratio such that $D/(M+1)$ is a prime integer number. f.e. if the record size is 32768, M+1 equals 32769, which can be factorized in terms of prime numbers as 3*3*11*331, consequently, D can be chosen 331. For 100 MHz, the input frequency obtained is 1.01013183975 MHz.

Once an input frequency is chosen, a minimal amount of samples / cycles is required, depending on how accurate the measurement needs to be carried out. The minimal number of samples is based on the following formula [14]:

$$N_{RECORD} = \left[\pi 2^{n-1}\left(Z_{\frac{\alpha}{2}}\right)^2\right]/\beta^2 \quad (7)$$

$$Z_{n,\alpha/2} = \sqrt{2}erfc^{-1}\left(1-(1-\alpha)^{2^{-n}}\right) \quad (8)$$

where β makes reference to the DNL error in LSB expected and α is the degree of confidence, which leads to the term $Z_{n,\alpha/2}$ used on the formula (7) and (8) to calculate the number of samples of our record. For n=14 bits, the values obtained for several values of β and α are summarized on the table I.

TABLE I. RECORD SIZE FOR DIFFERENT VALUES OF β AND α

Confidence	β=1	β=0.5	β=0.2	β=0.1
90 %	69642	178568	1741052	6264206
95 %	98867	395469	2471678	9886714
99 %	170778	683111	4269446	17077785

As we can see from the table I, the record size increases dramatically as the DNL error decreases. The measurements for this FADC have been done with a 95% confidence and β=0.2.

Once the record has been acquired, its histogram is evaluated, forming from the sine the characteristic bathtub function. A transformation must be applied in order to convert it to what would be linear-like. This operation can be calculated from the cumulative histogram function, and multiplying it by a transformation function such that the product is linear. From the linearized function, DNL and INL parameters can be extracted, in the same way as in a common density test [14].

4) Histogram-based Measurements.

Measurements based on histograms are a common way in nuclear physics to evaluate the performance and noise of electronics and detectors. In γ-spectroscopy, this is generally evaluated by performing the energy spectrum, which depicts the number of events taken within a certain energy interval. This way to make measurements contemplates a more realistic point of view, since the signals generated are pulses like the ones detected on the germanium. Besides, it is more integrated with part of the firmware for digital signal processing. This step has been implemented in order to observe the FADC Mezzanine behavior when detector-like pulse signals come into stage, and the main evaluated is the FWHM (Full-Width Half Maximum), a parameter closely related to the noise sigma by the relation (9).

$$FWHM = 2.35\sigma \quad (10)$$

As it was mentioned before, for the histogram measurements, the pulse generator BNC PB-4 based on NIM was preferred generating pulse-like waveforms with a constant rise-time and decay-time, set to 100ns and 50µs respectively.

The firmware requires two extra firmware components more to extract the energy and to build up the histogram. One block is used to extract the energy based on the pulse-height, passing it through a trapezoidal filter in order to catch easier the top peak. The second block, named as Histogram memory implements a 16k-sample memory in which all the possible energy values are stored in [4]. The expanded block diagram is shown in Fig.8.

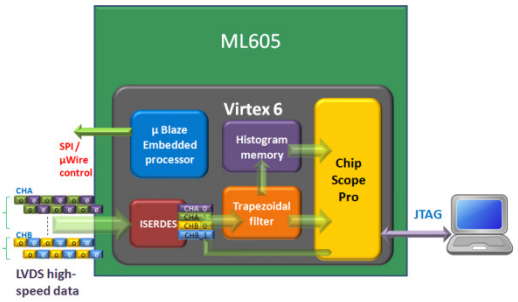

Fig. 8. Expanded firmware block diagram with the energy calculus and histogram memory. It is used to perform the energy resolution measurements.

IV. FADC MEZZANINE RESULTS

On this section, the results concerning the noise performance, ENOB, nonlinearities and energy are discussed.

1) Noise Performance Results

Noise results have been obtained with sampling frequencies of 100 and 200 MHz, on both channels. The procedure to calculate the noise basically consists in digitizing a signal without any input connected to it. The values then are monitored with the use of Chip Scope Pro and its histogram is extracted in Matlab. Although the FFT seems normally distributed, a slight term from the *1/f* noise is present on the first FFT samples. Table II synthesizes the results in terms of the noise standard deviation, assuming that it is white noise, The RMS noise voltage can be calculated as $V_{noise} = \sigma V_{LSB}$, knowing that $V_{lsb} = 122.6\ \mu V$, the RMS noise values are:

TABLE II. NOISE σ FOR DIFFERENT CHANNELS AT DIFFERENT SAMPLING FREQUENCIES

V_{noise} (RNS)	f_s = 100 MHz	f_s = 200 MHz
Channel A	327.32 μV	354.42 μV
Channel B	337.22 μV	373.12 μV

Based on the the RMS, just to take an example, at 100 MHz, for the channel A, the σ in ADC counts is 2.6699. If we calculate from this expression the SNR value according to the expression (1), the SNR is 66.69 dB.

2) ENOB Results

The ENOB has been calculated by driving sine waves at different frequency and different voltage. Then, separating the frequency components from the signal energy from the noise and distortion energy, SINAD, and therefore, ENOB can be calculated according to the formula (5). As we can see on the Fig.9. the ENOB increases as the input amplitude decreases. This fact is very important since, the n-th harmonic power decreases to the n-th power as the input amplitude decreases.

Obviously, the results contemplate the ENOB correction factor shown in (5).

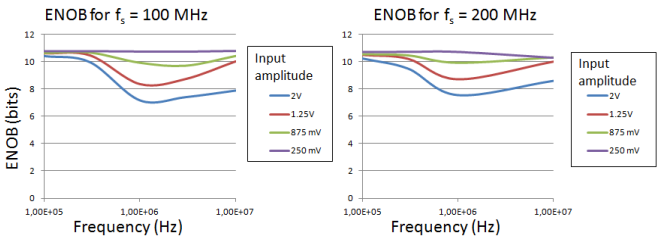

Fig. 9. ENOB curves across the frequency at different amplitudes. On the left it has been plotted the ENOB for a 100 MHz sampling rate while on the right the measurements are performed for 200 MHz.

If we compare the SNR and SINAD parameters, while the SNR calculated with the previous measurements gave 66.69 dB, the SINAD obtained at low frequencies, where the Agilent 3352A generator distortion is negligible was 66.35 dB. This fact points out the fact that FADC effectively does not introduce distortion.

3) DNL and INL Results

According to the procedure mentioned on the section III.3, both DNL and INL tend to increase with the sampling frequency , as shown on the Fig.10.

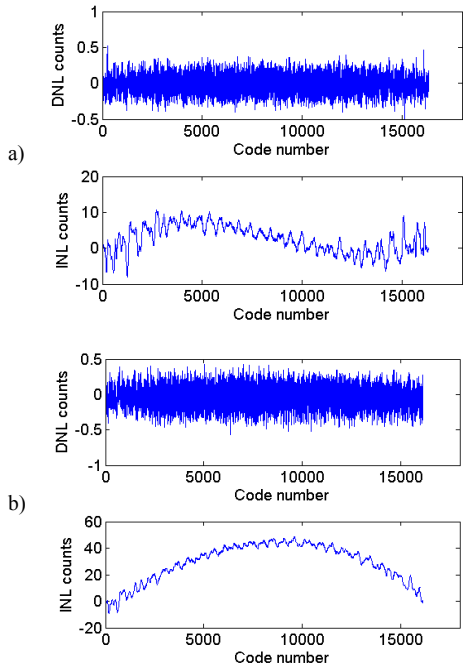

Fig. 10. INL and DNL curves taken at a) 100 MHz, and b) 200 MHz.

Nevertheless, the DNL with values around 0.25 LSB for f_s=100 MHz and 0.4 LSB for f_s=200 MHz, do not exceed the value ±1 LSB, showing that there are no missing codes.

4) Histogram Measurements

Finally, concluding with the results part, in order to perform the measurements, the tests have been taken at different amplitudes, or input energies, for which the crucial parameter is the FWHM.

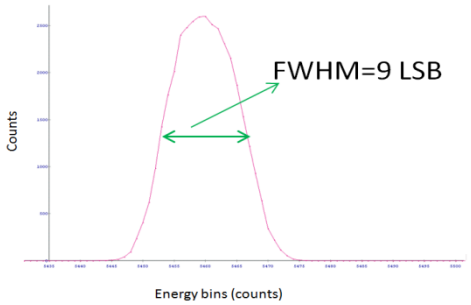

Fig. 11. Zoomed histogram for a 1.046 MeV energy.

From the Fig. 11. the resolution can be calculated from the energy bins if the channel energy is known. For this case, pulses with peak values 209 mV and 441 mV were generated, in energy, 1.046 MeV and 2.2 MeV, respectively. Since the histogram used contains 16.384 samples, and the energy bins fell on the samples 5462 and 11541, the measured FWHM in histogram counts was 9 LSB, equivalent to 1.723 keV. Although this energy resolution is compliant with the specifications demanded, the noise baseline still contains a σ in ADC counts equal to 2.6699. The reason why the resolution improves is due to the MWD filter, in which the noise performance is improved.

V. Conclusions

A comprehensive FADC mezzanine design has been detailed, gathering the FADC test bench with a configuration setup and the firmware requirements. Hence, the elaboration of an easy-testable device allows the measurement of the FADC mezzanine performance and its strong and weak points.

The results have shown a satisfactory behavior according to the functionality and dynamic range as well as the firmware and setup. However, the noise contribution must be studied more carefully, since the results according to the noise specifications, although not far from the specifications given, do not reach the ENOB 11.3 bits yet.

The noise and distortion measurements have shown that the board does not introduce extra distortion, hence, the ENOB can be calculated directly from the SNR assuming the distortion is negligible. Therefore, taking 11.3 effective bits, the SNR obtained is 69.8 dB, which implies a σ roughly around 1.85 counts. Recent noise measurements pointed out that the biggest noise contribution is due to the CFA AD8002 whose current spectral noise density seems to overcome the specified limits. A second prototype with an alternative analog stage, aiming to improved noise performance, is under study.

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